The development of a IGBT-based Tap Changer

by

Reinhart Fourie

Thesis presented in partial fulfilment of the requirements for the degree of Master of Science in Engineering at Stellenbosch University

Supervisor: Prof Hendrik du Toit Mouton
Department of Electrical & Electronic Engineering

March 2010

Declaration

By submitting this thesis electronically, I declare that the entirety of the work contained therein is my own, original work, that I am the owner of the copyright thereof (unless to the extent explicitly otherwise stated) and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

March 2010

Abstract

Voltage regulation on distribution networks has so far been done by means of mechanical tap changers. However, these tap changers are plagued by high maintenance costs due to the arcing caused while switching, which degrades both the contacts and transformer oil. The major advances made during the last decade with regard to semiconductor technology have led to the development of high power IGBTs. These high power IGBTs are capable of conducting currents up to 1 000 A, while the voltage over the IGBT reaches well over 3 000 V. Using these high power IGBTs to design and build a solid-state tap changer allows the tap changer to regulate the output voltage with higher accuracy and speed. The supporting hardware is also discussed, while the design is verified by the use of simulations and practical measurements conducted on a scale-model of the IGBT-based solid-state tap changer.

Opsomming

Spannings regulasie op distribusie netwerke word hedendaags verrig deur meganiese tap geskalde spanning reguleerders. Maar hierdie tap skakelaars word konstant beïnvloed deur oorvonking wat plaasvind tussen die kontakte wat hierdie kontakte beskadig en die transformator olie degradeer. Die laaste dekade het groot vordering getoon in halfgeleier navorsing wat gelei het tot die ontwikkeling van hoë drywing halfgeleiers. Die halfgeleiers of IGBTs kan strome so groot soos 1 000 A gelei terwyl die spanning oor die halfgeleier 3 000 V kan oorskry. Die gebruik van die hoë drywing halfgeleiers maak die pad oop vir die ontwerp en bou van 'n tap geskakelde reguleerder wat die uitree spanning akurater en vinniger kan reguleer. Die aanvullende hardeware is ook bespreek en die ontwerp is geverifieër deur middel van simulasies en deur praktiese metings wat geneem is op 'n skaal model van die hoogspanning spannings reguleerder.

Acknowledgements

I would like to thank the following person :

To My Lord and Saviour, Jesus Christ, for given me the talents and ability to complete this thesis.

To my study leaser, Prof. Mouton, for his guidance and input throughout the thesis.

To SANERI (South African National Energy Research institute), for the personal financial support for the entire duration of the thesis.

To all the fellow members of the PEG group for there support and assistance.

Contents

List of Figures

List of Tables

Nomenclature

Abbreviations

ADC	Analogue-to-digital converter
BOD	Break-over diode
FPGA	Field programmable gate array
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
LEM	Liaisons Electroniques-Mécaniques
MOV	Metal-oxide varistor
MV	Medium voltage
PC-board	Printed circuit board
PID	Proportional-integral derivative
PLL	Phase-lock-loop
PWM	Pulse width modulation
RAM	Random access memory
RMS	Root mean square
RTC	Real-time clock
RX	Receiver
TX	Transmitter

Circuit symbols

C	Capacitor
CO	contact
D	Diode
L	Inductor
R	Resistor
T	IGBT
S	Thyristor
SW	switch
Z	Zener diode

Units

°C	Degrees celcius
A	ampere
F	farad

H	henry
Hz	hertz
J	joule
K	kelvin
s	second
V	volt
VA	volt ampere
W	watt
Ω	Ohm

Other

a_I	Current ratio
a_T	Autotransformer transformation ratio
D	Duty cycle
E	Normalised switching energy [J/VA]
E_c	Common winding voltage [V]
E_p	Primary winding voltage [V]
E_s	Secondary or series winding voltage [V]
f	Frequency [Hz]
f_s	Switching frequency [Hz]
I	Current source
i_c	IGBT collector current [A]
i_D	Diode current [A]
i_{in}	Input current [A]
i_L	Output filter inductor current [A]
I_O	Peak inductor current [A]
i_o	Output current [A]
P	Active power [W]
P_{cond}	Conduction losses [W]
$P_s w$	Switching losses [W]
Q	Reactive power [VAR]
R	Resistance or reactance [Ω]
R_{th}	Thermal resistance [K/W]
S	Apparent power [VA]
T_a	Ambient temperature [°C]

T_c	Case temperature [°C]
T_j	Junction temperature [°C]
T_s	Period of switching frequency [s] or sink temperature [°C]
t_d	Time delay for switching of IGBT [s]
v_{ce}	Collector-emitter voltage [V]
v_F	Diode forward voltage [V]
v_{in}	Input voltage [V]
v_{Load}	Load voltage [V]
v_{out}	Output voltage [V]
v_s	Source voltage [V]
V_T	Peak tap voltage [V]
v_t	Tap voltage [V]
X	Admittance [Ω]
Δ_{i_L}	Ripple component of inductor current [A]
η	Efficiency
ζ	Damping ratio
ϕ	Phase shift [°]
ω	Radial frequency [rad/s]
ω_0	Fundamental frequency [rad/s]

Chapter 1

Literature overview

Apparatus used to regulate system voltages on distribution networks has been in use since 1890 [5] with the use of tap changers. Tap changers became an integral part of distribution power transformers and they are used to regulate the output voltage of the transformer. Regulation of the output voltage because it is necessary to compensate for the voltage drop over long-distance power lines.

Tap changers in general are divided into three categories [1], depending on the method of operation.

- Off-circuit tap changers: These operate only when the transformer is not energized, and thus they have very low maintenance requirements. Operated by means of a handle or wheel requires human interaction which results in no regulation of the output voltage.

- Off-load tap changer: These operate only when there is no load current flowing; the transformer allows the tap changer to operate while the transformer is energized. This allows the tap changer to switch between taps without interrupting the load for extended periods of time, as is the case with the off-circuit tap changer.

- On-load tap changers: The tap changer operates while the load current is flowing through the transformer; this allows it to regulate the output voltage to a certain limited degree. The only factor that limits the ability of the on-load tap changer to regulate the output voltage is the method of operation used for the tap changer. This issue is discussed later.

The specific type of tap changer that is implemented for the purpose of this report is an on-load tap changer, which is capable of regulating the load voltage while the full load current flows through the transformer.

Most on-load tap changers are mechanical in design, in that they use a motor that rotates a shaft or similar device to switch between the taps of

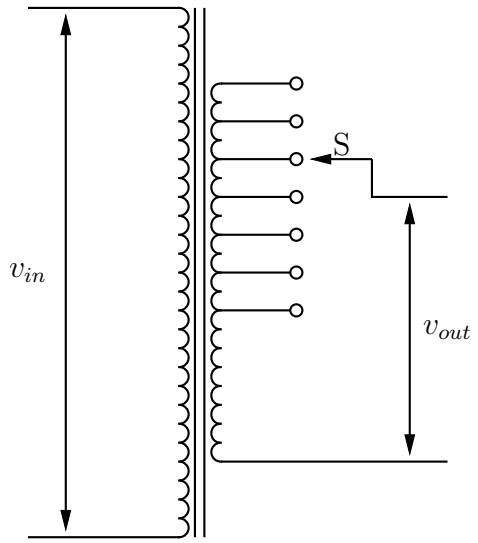

Figure 1.1: Basic layout of a single-phase linear tap changer [1].

the transformer. The basic layout of a single-phase mechanical tap changer is shown in Figure 1.1, connected to a step-down distribution transformer.

Moving switch S between the different taps of the transformer in Figure 1.1 changes the output voltage v_{out} by changing the turns ratio of the transformer. The single switch configuration arcs during operation from one tap to another, which degrades the transformer oil as well as the contacts of the tap changer. This drawback led to the development of the resistor and the reactor diverter switch assisted tap changer, which were introduced around 1936 [5]. These types of tap changer implement two selector switches and a diverter switch to minimize the arcing while switching between the taps. Figure 1.2 shows the layout of a resistive diverter switching tap changer with two selector switches.

The tap changer in Figure 1.2 shows the connection diagram of a tap changer on the primary winding of a transformer that has been fitted with a diverter switch. The tap changer uses the diverter switch to change the output from Tap 1 to Tap 2. Moving the diverter switch upwards connects the diverter switch to both contacts CO_1 and CO_2, before it breaks with contact CO_1. Moving the diverter switch up even further connects the diverter switch to contact CO_3. While the diverter switch is connected to both contacts CO_2 and CO_3, the two taps share the load current while resistors R_1 and R_2 limit the current flowing between the taps. Moving the diverter switch up even further allows the switch to disconnect from contact CO_2 before it connects to CO_4. The diverter switch stops moving after the switch has been disconnected from contact CO_3 and connects the output to the transformer through contact CO_4 only. Using a charged spring mechanism to move the diverter switch allows the change to take place in about 20 ms, which requires resistors R_1 and R_2 to be specified for short time durations.

Using the diverter switch to minimize the arcing while switching lowers the

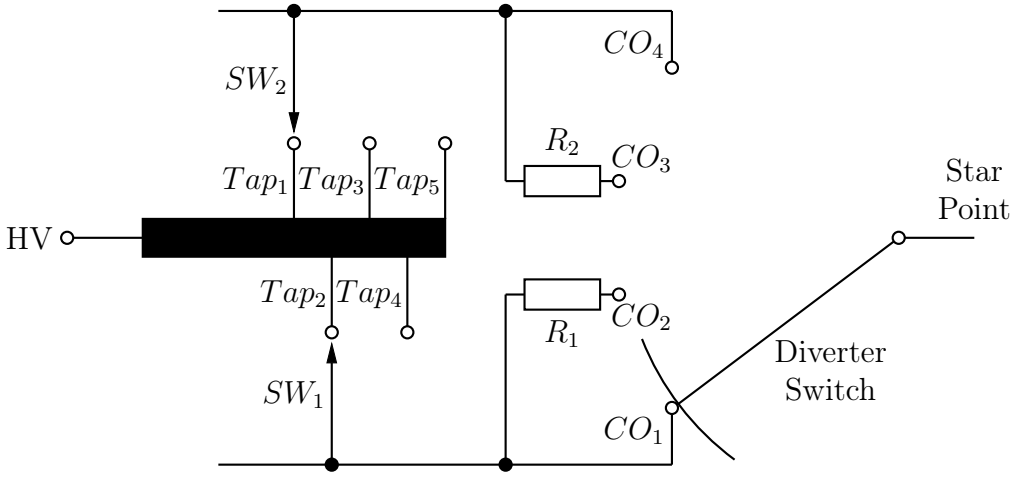

Figure 1.2: Layout of a diverter operated tap changer with two selector switches [1].

maintenance costs of the tap changer, but arcing still occurs. It is for this reason that tap changers are still maintenance intensive. Tap changers operated with the diverter switch, through either a resistance or a reactor, until vacuum operated interrupters were introduced in 1960 [5]. Vacuum interrupters isolate the arc created while switching from the oil inside the tap changer, thereby preserving the oil. These allow the tap changer to operate for longer time spans without requiring major maintenance.

The introduction of the silicon controlled rectifier or thyristor in 1963 [5] made it possible to use semiconductors in tap changers but the technology never reached a sufficiently mature level for commercial applications. The introduction of semiconductors resulted in the evlolution of three distinct types of tap changers for use in on-load tap changers:

- Full mechanical tap changer: These use only mechanical switches and contacts to switch between the taps of the transformer. Using vacuum switching to limit the amount of arcing still falls under this category.
- Electronically assisted mechanical or hybrid tap changer: These tap changers use thyristors in the diverter switch to minimize the arcing while switching.
- Full electronic tap changer or solid-state tap changer: Using only semiconductors to perform the switching offers numerous advantages over the previous two methods listed in Table 1.1 below.

The major differences between the three technologies are listed below in Table 1.1.

Attribute	Mechanical Tap changer	Hybrid Tap changer	Solid-state Tap changer
Maintenance	Regular contact and mechanical	Regular mechanical	No routine maintenance required
Cost	Fairly inexpensive	About the same as Mechanical	Considerably more expensive
Speed of response	One to 4 seconds per tap change	One to 4 seconds per tap change	One to two half-cycles per tap change
Tap step range	One tap per operation	Usually one tap per operation	Move between any taps per operation

Table 1.1: Major differences [5] between full mechanical, hybrid and solid-state tap changers.

As cost is the only disadvantage of the solid-state tap changer, it is still the most viable solution for use in tap changers due to the advantages it provides. Consequently, the rest of this report concentrates on solid-state tap changers.

Advances made in semiconductor technology in the last decade have led to the development of thyristors and insulated gate bipolar transistors (IGBT), which are capable of operating in medium voltage (MV) tap changers. The implementation of a thyristor into a solid-state tap changer is covered in the next section, and this is followed by the implementation of an IGBT into a solid-state tap changer.

1.1 Thyristor-based solid-state tap changer

The application of thyristors in tap changers has mostly been used in hybrid tap changers, with the thyristors replacing the diverter switch. But research has also been done on using thyristors in solid-state tap changers that are capable of switching from one tap to another in any order without using a diverter switch. The layout of such a solid-state tap changer is shown in Figure 1.3 [7]. It uses thyristors instead of a diverter switch to connect the taps of the transformer to the load.

The anti-parallel connection of the thyristors between each tap and the output allows the thyristors to conduct the output current independently of the current direction. The current direction or polarity also determines the switching direction of the tap changer. Switching from one tap to another depends on the polarity of the voltage and the current. Switching between taps in the incorrect order switches on two sets of thyristors at the same time, resulting in short-circuiting the taps of the transformer. Short-circuiting the transformer, furthermore large fault currents to flow through, thus damaging taps the thyristors, which is clearly not a desirable outcome.

The waveforms in Figure 1.4 [7] show in which direction they may be switched for the specific voltage and current polarities.

Voltages v_1, v_2 and v_3 are the voltages provided by the three different taps of the transformer together with the output current i_{out} which are all indicated on the circuit diagram in Figure 1.3. Switching the output from the second tap position at v_2 to the first tap position v_1 for positive output current i_{out} can only be done in the allowed up-switch windows indicated in Figure 1.4. Switching on thyristors S_{1_A} and S_{1_B} after switching off thyristor S_{2_A} and S_{2_B} reverse biases thyristors S_{2_A} with thyristor S_{2_B} switched off. Reverse biasing thyristor S_{2_A} allows the current through the thyristor to go to zero, while thyristor S_{1_A} conducts the output current.

Switching the thyristor-based solid-state tap changer in this manner allows the tap changer to regulate the output voltage as the input voltage changes. But the output of the tap changer while switching will not be a perfect sinusoid due to the hard switching between the taps. The output regulation range and accuracy of the tap changer are limited by the amount of taps provided by the transformer, in that fever taps result in a wider spread. While more transformer taps provide a narrower regulation accuracy, this comes at a cost, as more thyristors are needed for each tap.

The major advantage of using thyristors in this arrangement is that it makes available an arc free alternative to the mechanical tap changer, which is capable of jumping between multiple taps during one tap change cycle. The major disadvantage of thyristor-based tap changers is the fact that they still do not improve system stability. As they are dependent on the polarity of the

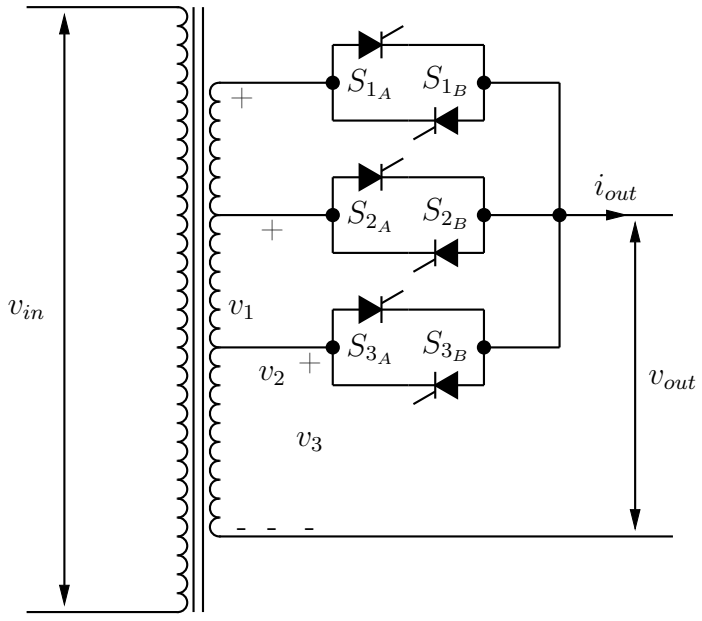

Figure 1.3: Layout of a thyristor-based solid-state tap changer.

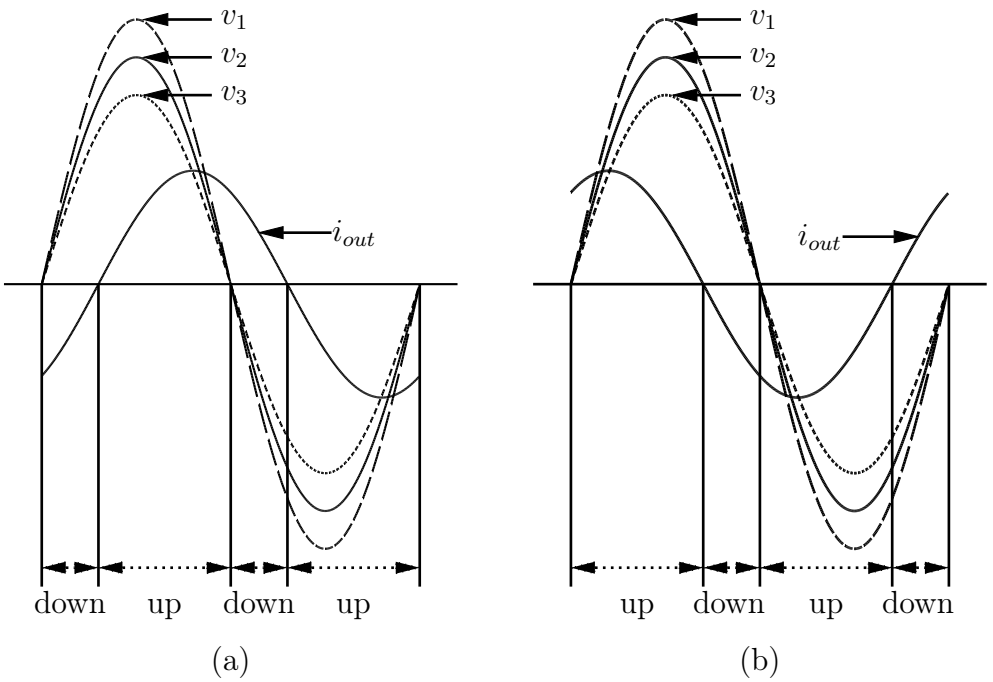

Figure 1.4: Waveforms indicating switching direction depending on voltage and current polarity;(a) Lagging power factor; (b) Leading power factor.

voltage and the current may, the tap changer may need to wait up to half a cycle to perform a tap change with power factors close to one. Furthermore, the thyristor-based tap changer is unable to perform sudden voltage rise and dip compensation.

Another disadvantage which has to be counted for is the voltage limit of the thyristors. This voltage limit presents problems during fault conditions on the load side where the output voltage drops close to zero and causing the thyristors to be damaged due to over voltages. One method to overcome this problem is to connect multiple thyristors in series so that the voltage over the thyristors are divided between the thyristor during fault conditions.

Using IGBTs allows the tap changer to perform voltage compensation, thus improving system stability with a change in circuit layout. This is a result of the ability of the IGBT to switch-off, while the output current flows through the IGBT.

The next section looks at an implementation of IGBTs into a solid-state tap changer.

1.2 IGBT-based solid-state tap changer

Using IGBTs in a tap changer requires a different approach because the IGBTs have only two switch states, i.e. either on or off. As there is thus no in-between

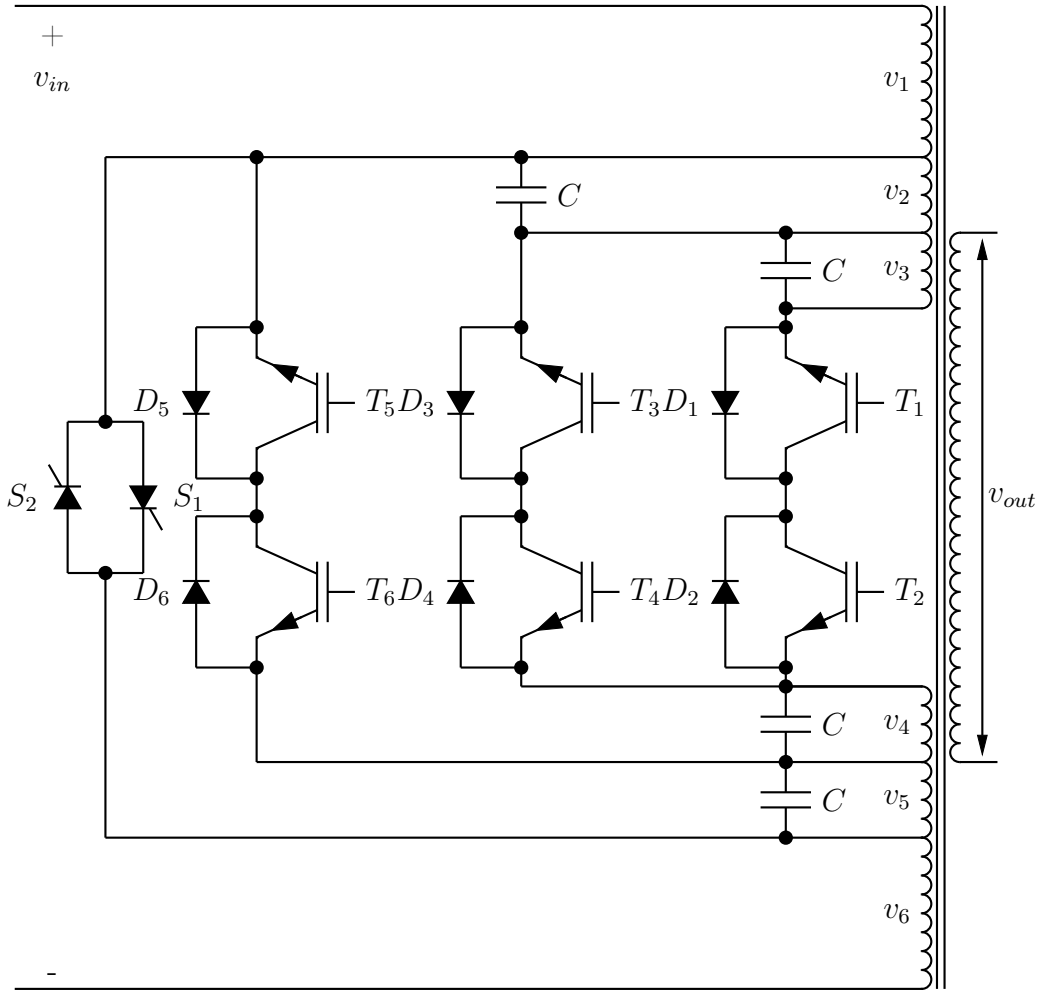

Figure 1.5: Basic circuit layout of one of the phases of a solid-state tap changer using IGBTs.

on state, and as IGBTs are able to switch-off while conducting current allows them to be pulse width modulated (PWM) at frequencies of up to 200 times higher than the fundamental of 50 Hz. Changing the duty cycle of the PWM from 0 to 100% allows the tap changer fitted with IGBTs to regulate the output voltage with a higher degree of accuracy than would be possible with an thyristor-based solid-state tap changer.

Implementing IGBTs for use in tap changers on a MV transformer raises one major problem, which is the low blocking voltage of current high voltage IGBTs. The highest blocking voltage achievable by any IGBT at the time of this writing is 3 600 V peak with a 6 500 V Eupec IGBT [8]. The 3 600 V rating of the IGBT is the highest voltage at which the IGBT can operate, while the 6 500 V rating is the maximum voltage which the IGBT can block while switched off permanently. But the blocking voltage is lower than the 11 000 V_{RMS} of a standard MV grid. Consequently, using the taps provided by

a distribution transformer that is used for mechanical tap changers, permits smaller voltages over the IGBTs. These taps provide voltages that are low enough so that 1 700 V IGBTs can be used, which currently present the lowest switching losses and the highest switching frequency out of all the high voltage IGBTs available.

A connection scheme that connects the IGBTs between the taps of the distribution transformer is shown in Figure 1.5 [9].

The circuit diagram in Figure 1.5 shows three IGBT pairs with IGBTs T_1 and T_2 forming the right pair, and T_3 and T_4 the middle pair, while T_5 and T_6 form the left IGBT pair. Each IGBT also has an anti-parallel diode connected over the IGBT. The connection of the IGBT pair together with the diodes forms bi-directional switches, thus allowing current to flow in both directions while switching. Thyristors S_1 and S_2 form a bypass switch or crowbar that protects the IGBTs from over-voltage and over-current situations by connecting the lowest tap v_6 with the highest tap v_1, thus bypassing the IGBTs. Connecting the IGBTs and thyristor to the primary side provides a major advantage by lowering the current the semiconductors have to conduct. Lowering the current reduces the switching losses even more, and it further lowers the fault current, which has to be conducted by the IGBTs during fault conditions.

The capacitors between the taps are used to provide an alternative current path for the reverse recovery current of the diodes which does not go through the transformer.

Table 1.2 shows the operating parameters [10] for the IGBT-based solid-state tap changer shown in Figure 1.5.

Operating the IGBT-based solid-state tap changer in Figure 1.5 under normal parameters is done through the IGBTs. Operating the left pair of IGBTs T_5 and T_6 connects tap v_1 to the combination of taps v_5 and v_6 added together. This connection changes the turns ratio of the primary winding of the transformer. Using PWM allows the output voltage of the secondary tap to be controlled continuously for the voltage range in which the IGBT pair of T_5 and T_6 can operate. In the event that the output voltage needs to be controlled

Description	**Value**
Input voltage	10 kV_{RMS}
Output voltage	400 V_{RMS}
Power rating	500 kVA
Input current	28.867 A_{RMS}
Output current	721.687 A_{RMS}
Tap voltage	250 V_{RMS}

Table 1.2: Operating parameters for a three-phase IGBT-based solid-state tap changer designed for the European market.

beyond the range provided by the leftmost IGBT pair, the other IGBT pairs are used. Using these other IGBT pairs changes the turns ratio of the primary winding of the transformer. This attribute of the connection of the IGBT pair to the different taps allows the tap changer to regulate the output voltage with a wider output voltage range that would be possible if only a single pair of IGBTs were used.

The major advantages and disadvantages of the IGBT-based solid-state tap changer in Figure 1.5 are the following :

- Implementing the IGBTs on the primary side of the distribution transformer allow low current IGBTs to be used.
- The low tap voltage of 250 V allows low voltage IGBTs to be used.
- Using PWM to control the switching of the IGBTs allows the controller to control the output of the transformer continuously.
- One possible problem is the effect that the switching has on the windings of the transformer. Switching at high frequencies generates voltage spikes, which degrades the insulation on the windings leading to unforeseen failure of the transformer, earlier than expected.
- The implementation of the IGBTs in the specific layout requires 2 more IGBTs for each tap increase, which greatly increases the cost of such a tap changer.
- Increasing the number of taps per phase also increases the control cost in that more can go wrong.

The next section compares the advantages and disadvantages of the IGBT-based tap changer with those of the thyristor-based tap changer.

1.3 Comparison of IGBT-based and thyristor-based solid-state tap chnagers

Comparing the advantages and disadvantages of the IGBT-based solid-state tap changer with those of the thyristor-based tap changer shows clearly that the IGBT-based solid-state tap changer is superior to the thyristor-based tap changer for the following reasons :

- Continuous voltage regulation: The IGBT-based solid-state tap changer is capable of regulating the output voltage continuously.

- Semiconductor count is less: Using fewer IGBTs between the taps allows the IGBT-based solid-state tap changer to be more cost-effective than a thyristor-based solid-state tap changer when using a large number of taps.
- Voltage over switches: The voltage that the IGBTs must be able to handle is not limited by the voltage provided by the taps. In the event that a fault occurs on the load side of the transformer and the IGBTs are located on the secondary winding, the voltage difference over the IGBTs will be significantly larger than which the IGBTs are designed for. This requires the use of extra equipment, such as a bypass switch consisting of thyristors and surge suppressors that protect the IGBTs from high voltages. This has a negative impact on the cost of the IGBT-based solid-state tap changer.
- Maintenance: Comparing the solid-state tap changers presented here with a mechanical tap changer allows one large factor to stand out. The maintenance on a solid-state tap changer is close to nil because there are no mechanical moving parts and because no arcing occurs while switching.

Nonetheless, the IGBT-based solid-state tap changer does present a couple of disadvantages, which leave room for improvement. This is discussed in the next section, which looks at the scope of this thesis.

1.4 Scope of thesis

The object of this thesis is to design and implement an IGBT-based solid-state tap changer with the ratings shown in Table 1.3.

Description	**Value**
Input voltage	6 351 V_{RMS}
Output voltage	6 351 V_{RMS}
Power rating	63 kVA
Output current	100 A_{RMS}
Tap voltage	635.1 V_{RMS}
Switching frequency	10 kHz

Table 1.3: Required ratings for the IGBT-based solid-state tap changer in this thesis.

The IGBT-based solid-state tap changer, which is more simply referred to as 'the IGBT-based tap changer' in the following chapters of this thesis, will be

connected to the output of commercially manufactured voltage regulator. The voltage regulator consists of an autotransformer connected to a mechanical tap changer. The IGBT-based tap changer will be designed to be an add-on to the voltage regulator without altering the internal connections of this voltage regulator. Essentially, the IGBT-based tap changer will replace the mechanical tap changer by delivering the regulated output voltage to the load.

1.5 Thesis outline

This section lists the chapters that make up this thesis together with a brief description of each.

- Chapter 2 looks at the topology used for the IGBT-based tap changer together with the switching scheme and controller used.
- Chapter 3 examines how the IGBT-based tap changer operates, with a particular emphasis on how the voltages and currents flow through the different semiconductors.
- Chapter 4 derives the equations needed to calculate the losses, as well as presenting the design of the heat sink and passive components.
- Chapter 5 considers the implementation of the design equations for a specific IGBT model, as well as the value calculations for the passive components.
- Chapter 6 looks at the supporting hardware that is used either to drive the IGBTs or to measure the voltages and currents of the IGBT-based tap changer and other hardware.
- Chapter 7 scrutinises the design of the feedback controller that is required to control the IGBT-based tap changer so that it regulates the output voltage of the tap changer.
- Chapter 8 presents the results of the simulations conducted to verify the design of the IGBT-based tap changer.
- Chapter 9 focuses on the practical measurements conducted on a scale IGBT-based tap changer that was built to verify that the design is practically viable.
- Chapter 10 provides flow diagrams of the software implemented into the controller that has been used to control the scale IGBT-based tap changer.
- Lastly, Chapter 11 summarises the important aspects raised in the preceding chapters and presents the relevant conclusions of this thesis.

Chapter 2

Outline of the IGBT-based tap changer

The aim of this chapter is to provide a brief outline indicating the key components that make up the IGBT-based tap changer, together with a brief explanation of each. An in-depth analysis of the different components occurs throughout the subsequent chapters.

Below is a brief outline of this chapter, together with a summary of what will be covered in each section.

- Implementation of the AC-chopper: The AC-chopper chosen in Chapter 1 forms the bases of the IGBT-based tap changer. This section looks at how the AC-chopper is adapted into the IGBT-based tap changer to operate at voltages higher than those that can be reached by the normal AC-chopper.

- Key components: Each of the components discussed in this section is vital during the operation of the IGBT-based tap changer.

- Switching scheme: Switching the IGBTs used in IGBT-based tap changers in the correct order allows these tap changers to operate without causing damage to the IGBTs while they are regulating the voltage delivered to the load. This section looks at the switching scheme that has been implemented to ensure the safe operation of the IGBT-based tap changer.

- Control method: Regulating the load voltage requires the use of a feedback controller. This adjusts the duty cycle of the IGBT-based tap changer in order to regulate the load voltage.

The next section,then, starts by investigating the implementation of the AC-chopper in the IGBT-based tap changer.

2.1 Implementation of the AC-chopper

The AC-chopper[2] as discussed in Chapter 1 consists of four IGBTs T_1 to T_4, with their respective anti-parallel diodes D_1 to D_4 shown in Figure 2.1. The four IGBTs connect in series over the source v_s terminals. The output filter consisting of inductor L_O and capacitor C_O connects between IGBTs T_2 and T_3 and the load. Inductor L_i represents the inductance of the line between the AC-chopper and the source. Capacitor C_i forms an input filter, while capacitor C_l forms a snubber capacitor.

There is one significant problem with implementing the AC-chopper for use in the IGBT-based tap changer. Connecting the IGBTs to the source, as shown in Figure 2.1, forces the IGBTs to block the entire source voltage during operation. This is not a problem for applications between 230 V and 1 200 V, since most IGBTs available are capable of operating at these voltages. Higher voltage IGBTs can also be used but then the switching losses generated by these IGBTs will be too high to make the design a viable solution. Current IGBT technology forces the implementation of the AC-chopper to be altered to allow the use of lower voltage IGBTs.

However, altering the normal layout shown in Figure 2.2.(a) of the AC-chopper in order to utilise lower voltage IGBTs means adding a further voltage source. Setting the voltage of the additional voltage source to one-tenth that of the source voltage allows the voltage difference between the two sources

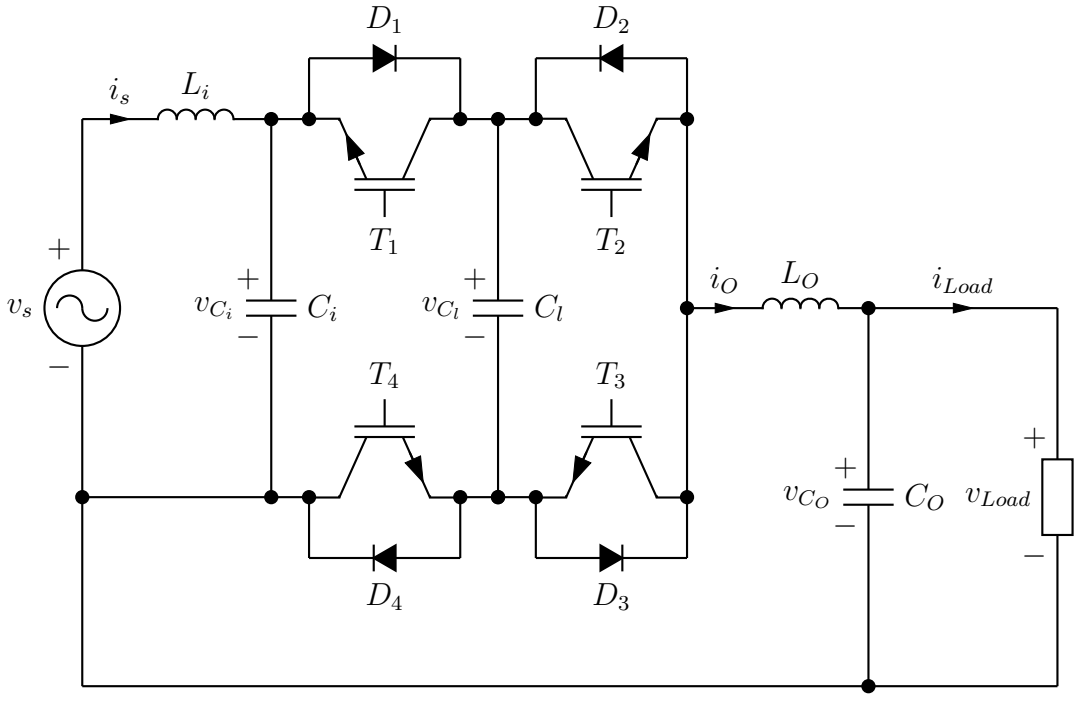

Figure 2.1: Circuit diagram of the AC-chopper [2].

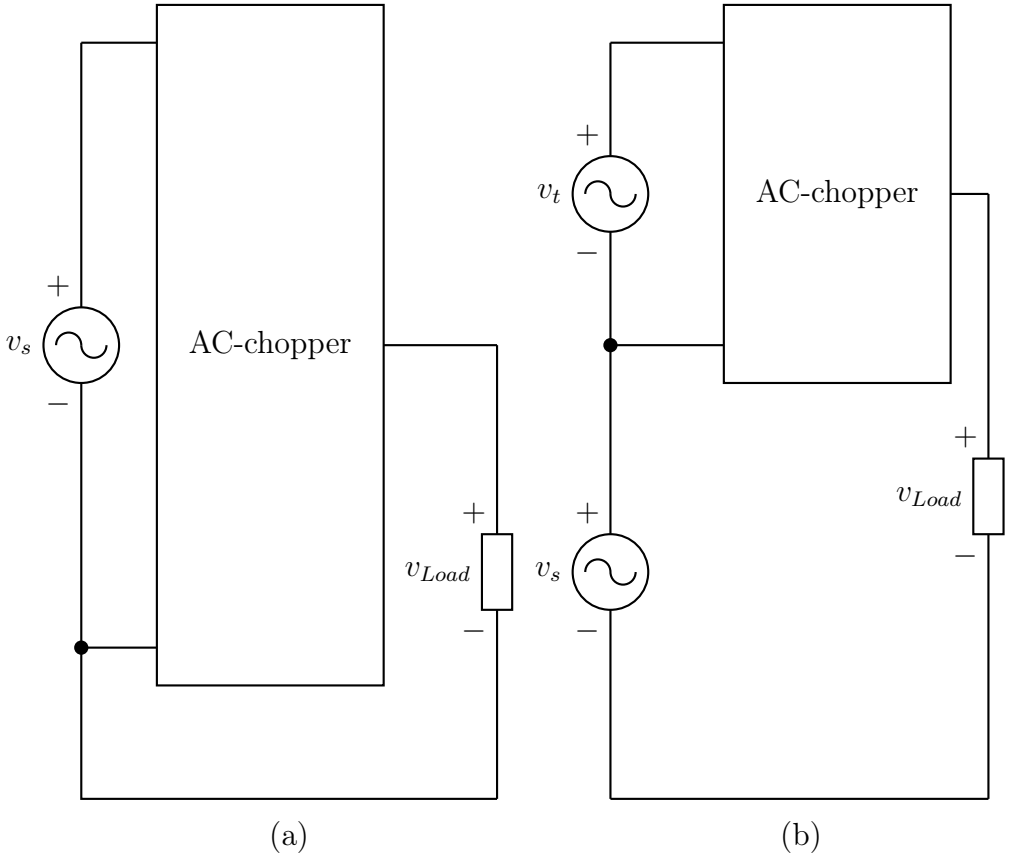

Figure 2.2: Circuit diagram showing how the AC-chopper is implemented for use on an autotransformer; (a) The AC-chopper connected directly to the terminals of the source; (b) The AC-chopper connected between the input and tap output of a autotransformer.

to be significantly lower than the source voltage alone. Connecting the AC-chopper directly to the source voltage and the additional voltage source shown in Figure 2.2.(b) allows the voltage seen by the IGBTs to be lower, although the source voltage is still very high.

Implementing an autotransformer to provide the additional voltage source is the most cost-effective solution.

The final implementation of all components required for the IGBT-based tap changer is shown in Figure 2.3.

With the AC-chopper connected to the source and the output of the autotransformer, the voltage over the AC-chopper is much lower than the nominal rated voltage v_{in}. The lower voltage that the AC-chopper will need to switch allow lower voltage IGBTs to be used resulting in higher switching frequencies. These in turn reduce the inductance of the output filter inductor L_O and thus decrease the physical size of the inductor. The filter capacitors C_1 and C_2 as well as the snubber capacitor C_s also benefit from the reduced voltage over the

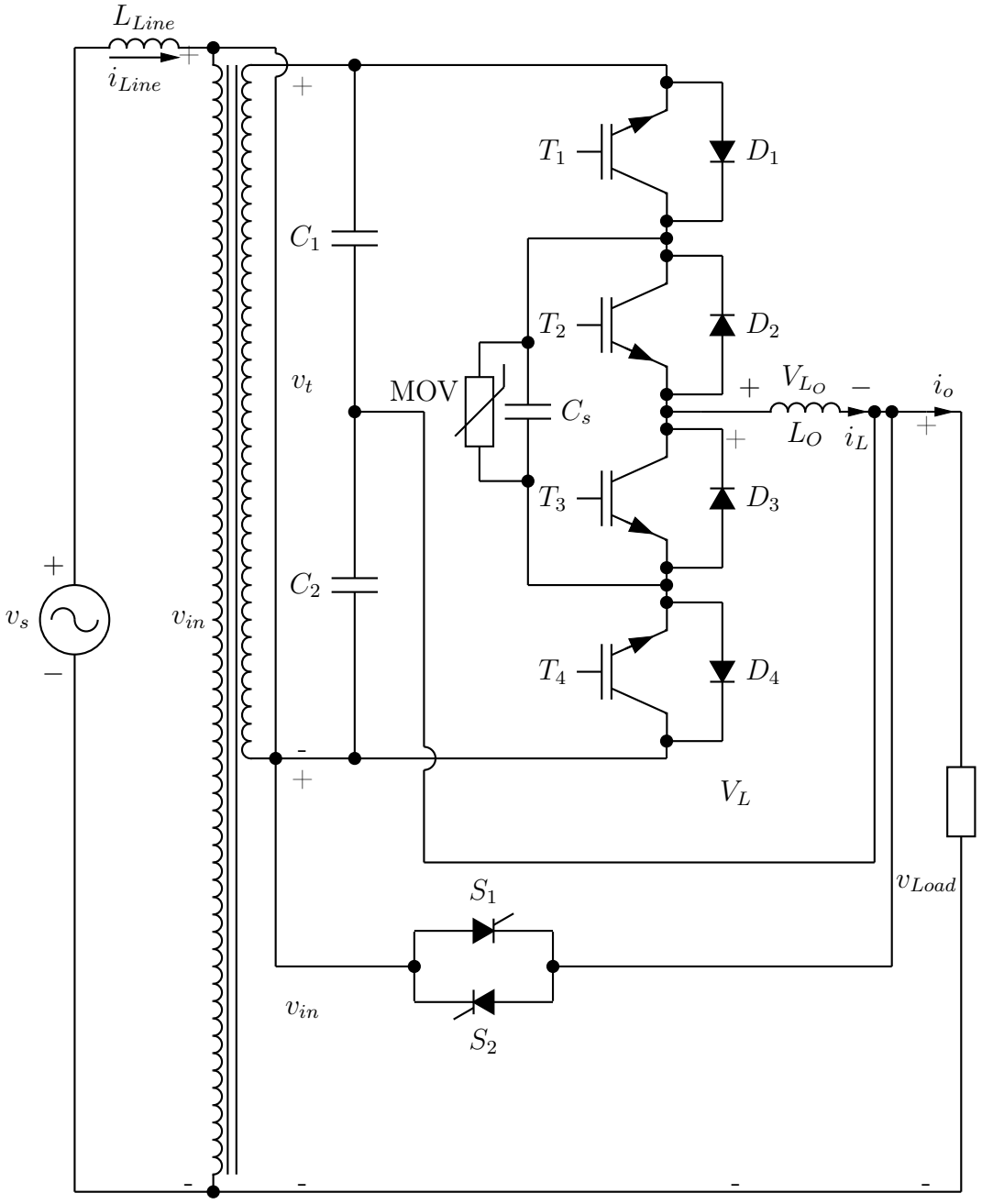

Figure 2.3: Circuit diagram of all the components used for the IGBT-based tap changer.

AC-chopper, as the voltage rating of these capacitors can then be significantly lower.

2.2 Key components

This section looks at all the components required by the tap changer shown in Figure 2.3 to operate. It will not be possible for the tap changer to operate if any of these components fail. In the list of the key components below, a brief overview of each component is given.

- Bi-directional switches: IGBTs T_1 to T_4 and diodes D_1 to D_4 are used in pairs of two, thus forming two bi-directional switches. These switches are the main components in the tap changer.
- Filter elements: The filter consisting of capacitors C_1 and C_2 together with output inductor L_O, form both an input and output filter in one.
- Snubber capacitor: The snubber capacitor C_s is used to provide an alternative current path for the inductor current during the dead time of the switching scheme.
- Bypass switch: The bypass switch, consisting of thyristors S_1 and S_2 is used to bypass the AC-chopper, thereby providing over-voltage and over-current protection for the IGBTs.
- Autotransformer: The autotransformer provides the second voltage source required by the AC-chopper.
- MOV: The metal-oxide-varistor (MOV) connected in parallel with snubber capacitor C_s protects the snubber capacitor from voltages higher than those for which it is designed for.

The following sections look at each the above-mentioned key components in more detail, starting with the IGBTs and finishing with the autotransformer.

2.2.1 Bi-directional switches

Connecting IGBTs T_1 to T_4 together with their respective anti-parallel diodes D_1 to D_4 in the configuration as shown in Figure 2.3 forms two bi-directional switches. The top bi-directional switch consists of T_1,T_2,D_1 and D_2, while T_3,T_4,D_3 and D_4 form the bottom bi-directional switch. Each of these switches conducts the inductor current i_L in either positive or negative current directions, independently of the voltage magnitude and phase shift between the input voltage v_s and load current i_o. The positive inductor current that flows through the top bi-directional switch flows through D_1 and T_2, as indicated in Figure 2.4.(a). The negative inductor current that flows through the top bi-directional switch flows through D_2 and T_1, as shown in Figure 2.4.(b). Figures 2.4.(c) and 2.4.(d) show the current flow through T_3, T_4, D_3 and D_4 for the positive and negative inductor currents respectively.

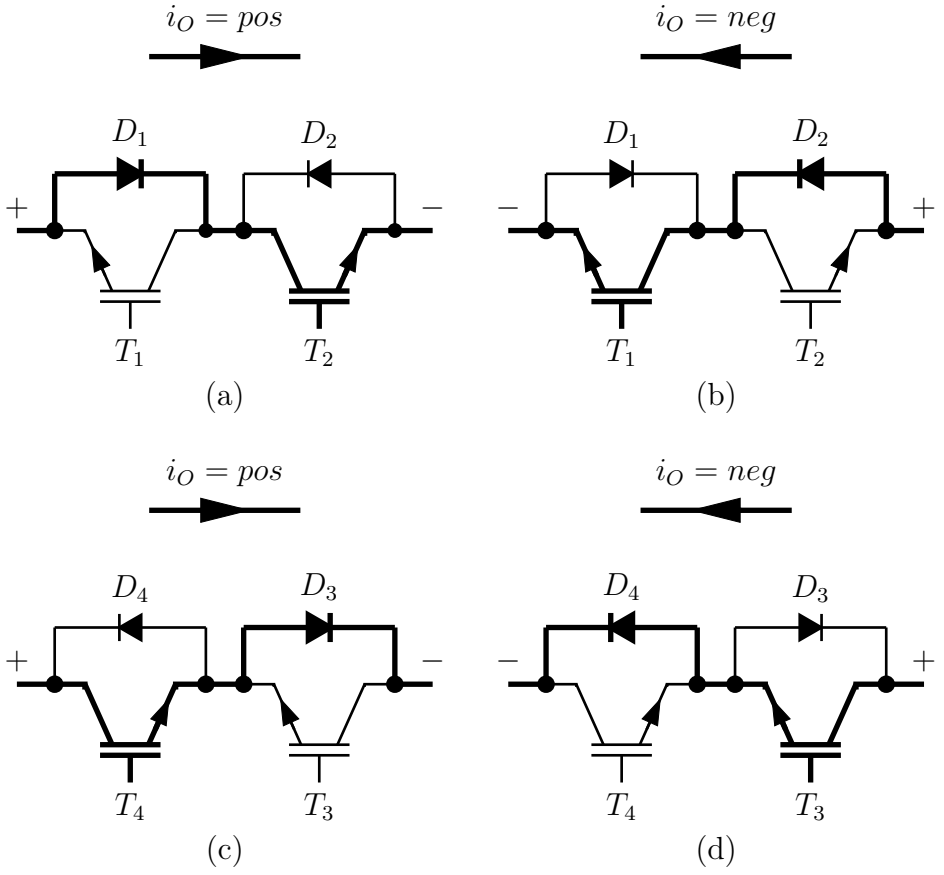

Figure 2.4: Current flow through the bi-directional switches: (a) IGBTs T_1 and T_2 conducting positive output current i_O; (b) IGBTs T_1 and T_2 conducting negative output current i_O; (c) IGBTs T_3 and T_4 conducting positive output current i_O; (d) IGBTs T_3 and T_4 conducting negative output current i_O.

Chapter 3 performs an in-depth analysis of the current change that occurs from one bi-directional switch to another and is thus not discussed further in this chapter. The switching order of the IGBTs is controlled by the switching scheme, which is discussed in section 2.3 of this chapter.

2.2.2 Filter elements

Filtering of the switching harmonics is accomplished by making use of capacitors C_1 and C_2 together with inductor L_O, as shown in Figure 2.3. This combination allows the ripple component of the inductor current i_L to flow unrestricted through the bi-directional switch, which is on at that specific time.

Figure 2.5.(a) shows the path that the ripple component of the inductor current will take when the top bi-directional switch is on. Figure 2.5.(b) shows the path of the ripple current when the bottom bi-directional switch is on.

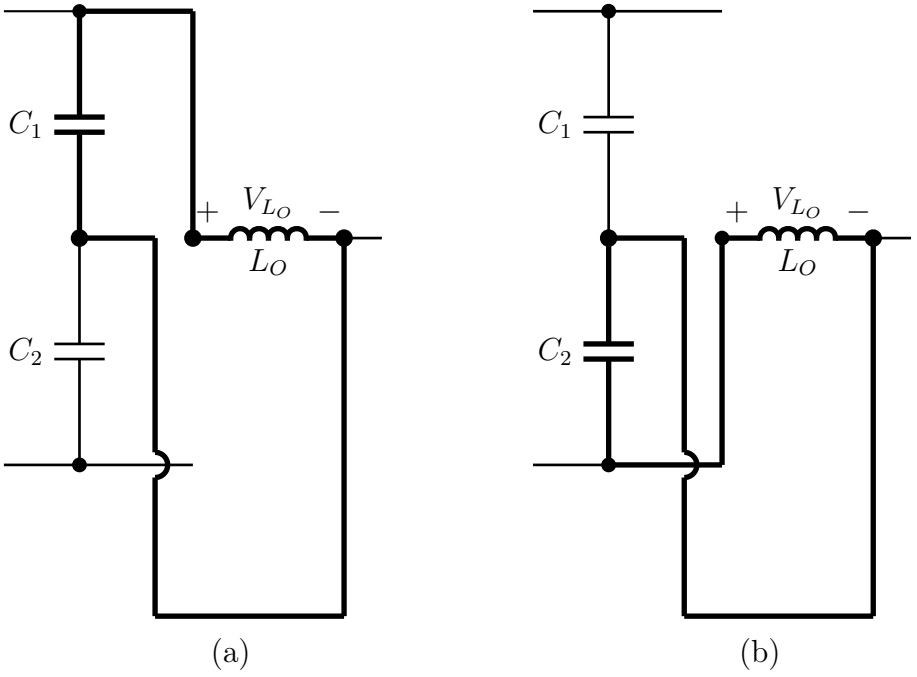

Figure 2.5: Current path of the ripple current flowing through inductor L_O; (a) Inductor ripple current flowing through top bi-directional switch; (b) Inductor ripple current flowing through bottom bi-directional switch.

The ripple current direction can be either positive or negative through the bi-directional switches.

Connecting the output filter inductor i_L to the filter capacitors C_1 and C_2, in the manner as depicted in Figure 2.5, creates an alternative path for the ripple component of the inductor current of inductor i_L to flow. This path forms the shortest route for the ripple current to flow, resulting in most of the ripple current flowing through the capacitors instead of through the autotransformer and the network. Thus not exposing the autotransformer and the network to the switching harmonics of the AC-chopper.

2.2.3 Snubber capacitor

Snubber capacitor C_s provides an alternative path for the inductor current i_L in the two situations listed below.

- During dead time: The snubber capacitor conducts the inductor current during the dead time period of the switching scheme.
- During loss of power to the controller or the IGBT driver circuits : If power is lost to either the controller or the IGBT driver circuit, then all the IGBTs switch-off. In this case, the snubber capacitor provides an alternative current path for the inductor current to flow.

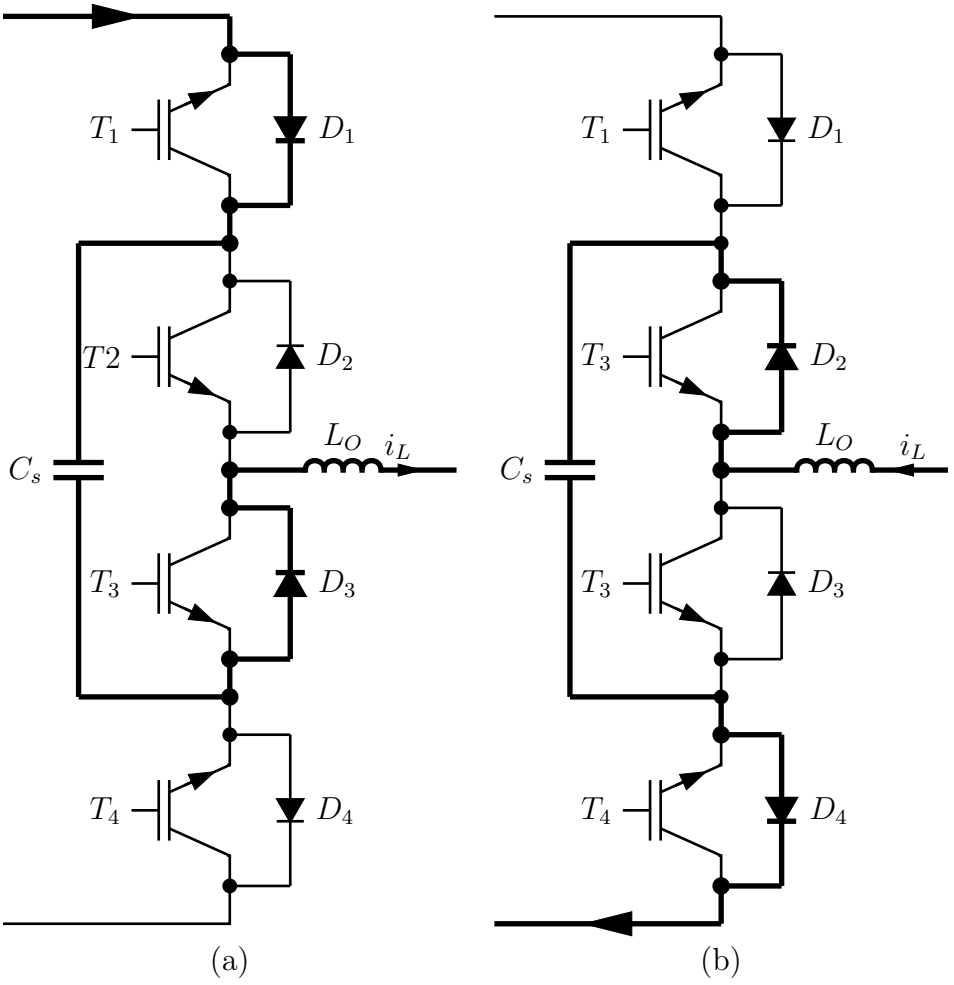

Figure 2.6: Current path of inductor current i_L for either situations; (a) Positive inductor current; (b) Negative inductor current.

The current paths for both positive and negative inductor current directions are shown in Figures 2.6.(a) and 2.6.(b) respectively.

A metal-oxide-varistor (MOV) is connected in parallel with the snubber capacitor in order to prevent the capacitor from reaching dangerous voltage levels. The MOV will start to conduct current when the capacitor reaches the MOVs break-through voltage, preventing the capacitor from being damaged due to over-voltage.

2.2.4 Bypass switch

The bypass switch consisting of thyristors S_1 and S_2 connects the input to the autotransformer and the output to the load as shown in Figure 2.3. This parallel connection allows the bypass switch to act as a protection mechanism for the AC-chopper. Protecting the IGBTs from over-voltage and over-current

conditions makes the bypass switch a vital component in the IGBT-based tap changer. The two protection methods are discussed briefly below.

2.2.4.1 Over-voltage protection

Protecting the AC-chopper from over-voltage situations is vital since the IGBTs are voltage sensitive; any voltages higher than the rated voltage of the IGBTs can potentially damage these. The bypass switch protects the IGBTs from voltages higher than the tap voltage v_t in Figure 2.3, which the IGBT switches. Two methods are used to turn on the thyristors in the bypass switch to perform the over-voltage protection.

- Active protection: Measuring the input voltage allows the controller to detect whether the input voltage is reaching dangerous levels; if this is the case, then a control signal activates the bypass switch before the IGBTs are damaged.
- Passive protection: Implementing break-over diodes to turn on the thyristors in the bypass switches provides a passive protection mechanism. The application of break-over diodes provides a failsafe method for performing the over-voltage protection since no control signal is required. This method is discussed in more detail in Chapter 6.

2.2.4.2 Over-current protection

Protecting the IGBTs from high currents is very important since conducting higher currents than those for which the specific IGBTs are rated, can potentially damage them. Over-current protection is accomplished by means of the same method as used above for over-voltage protection, namely, by switching on the thyristors in the bypass switch. An over-current situation is detected by two different methods, either by the output current measurement thats is conducted by the controller or through fault signals generated by the IGBT driver boards.

Measuring the voltage rise over the collector-emitter terminals of the IGBTs as the current rises through the IGBTs allows the IGBT driver board to determine if the IGBT is conducting more current than that for which it is rated. If the IGBTs are conducting more current than their ratings permit, the IGBT driver boards will send a fault signal to the controller board, alerting the controller board of the situation.

The controller activates the bypass switch if either the output current reaches the limit or a fault signal is received from an IGBT driver board.

If large fault currents are caused by an unknown disturbance, the controller must activate the bypass switch before the current through the IGBTs reaches the limit of the IGBTs. Consequently, the controller must be fast enough to

perform the over-current protection, which can be accomplished by means of a field-programmable-gate-array (FPGA) controller.

2.2.5 Autotransformer

The autotransformer performs one simple yet vital role in providing the additional higher voltage needed by the AC-chopper. An autotransformer is much smaller than a distribution transformer of the same rating, since the autotransformer only transforms the power needed to provide the higher tap voltage.

The autotransformer used in this application is capable of reversing the output of the transformer. Using the reversing switch allows the series winding to be connected in either a boosting or bucking series winding, depending on the connections. Connecting the input voltage v_{in} to the bottom terminal of the series winding configures the autotransformer in a boosting[11] configuration, shown in Figure 2.7.(a). Connecting the input voltage v_{in} to the top terminal of the series winding configures the autotransformer in a bucking[11] configuration, shown in Figure 2.7.(b).

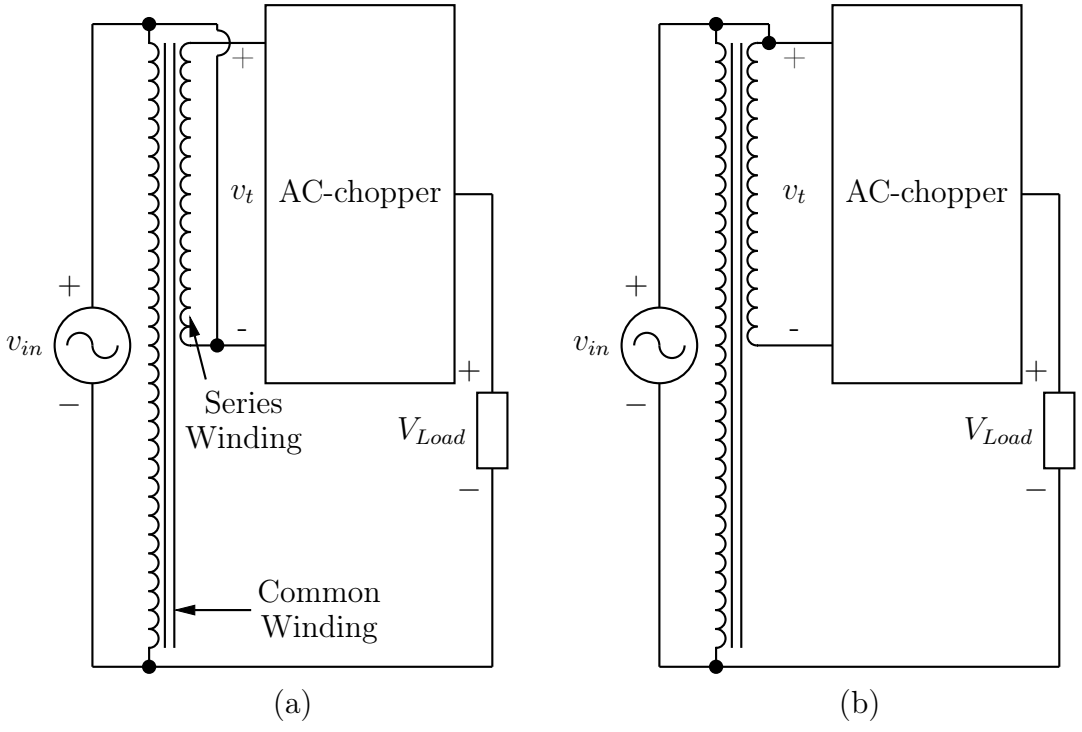

Figure 2.7: Autotransformer configurations; (a) Boosting configuration; (b) Bucking configuration.

2.3 Switching scheme

The switching scheme used to control the IGBT-based tap changer is based on three integrated principles. Implementing pulse width modulation (PWM) together with dead time allows the IGBT-based tap changer to regulate the load voltage, but this can only be done if the IGBTs' are commutated correctly.

Regulating the load voltage requires the duty cycle of the PWM to be adjusted while the IGBT-based tap changer is in operation. Changing the duty cycle of the PWM from 0% to 100% allows the IGBT-based tap changer to adjust the load voltage to be between the input voltage and the series winding voltage. Setting the duty cycle to 10% in Figure 2.8.(a), to 50% in Figure 2.8.(b) and to 90% in Figure 2.8.(c) results in the following load voltages for the respective duty cycles.

$$\begin{aligned} v_{Load} &= v_{in} + 0.1v_t \qquad (duty\ cycle = 10\%) \\ v_{Load} &= v_{in} + 0.5v_t \qquad (duty\ cycle = 50\%) \\ v_{Load} &= v_{in} + 0.9v_t \qquad (duty\ cycle = 90\%) \\ v_{Load} &= v_{in} + d\ v_t \qquad (for\ any\ duty\ cycle) \end{aligned} \tag{2.3.1}$$

Due to the non-ideal operation of the IGBTs, and to prevent them short-circuiting the autotransformer, requires that dead time must be implemented.

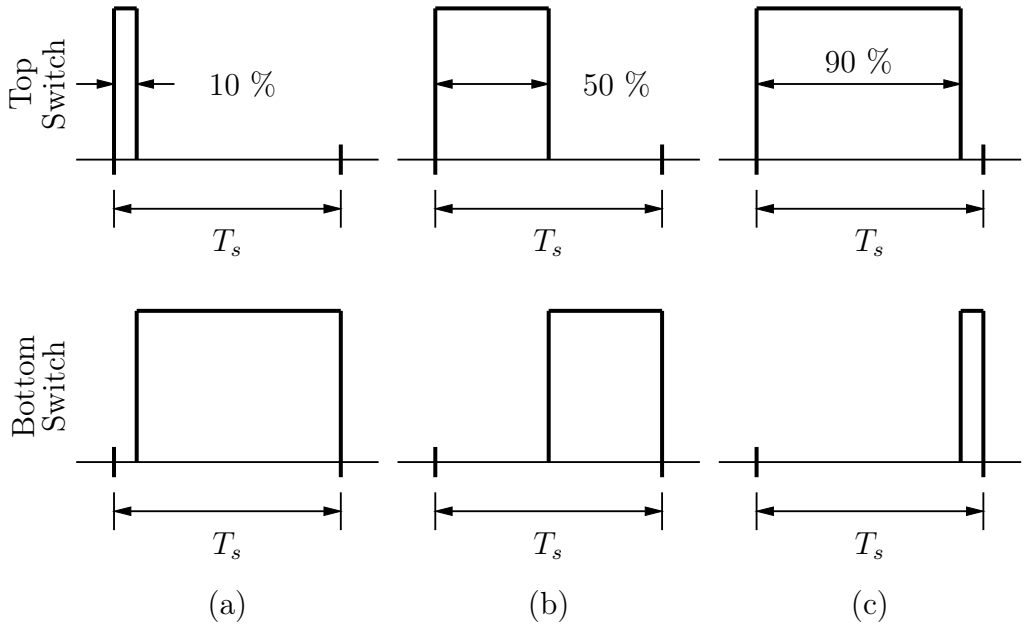

Figure 2.8: Gating signals for top and bottom bi-directional switches with T_s the period of the switching frequency; (a) 10 % Duty cycle; (b) 50 % Duty cycle; (c) 90 % Duty cycle.

Ideal IGBT operation requires the IGBTs to switch-off completely directly after the gating signal has been removed. But IGBTs unfortunately do not switch-off in this manner; instead, they only begin to switch-off after a short time of delay around 1 μs. Furthermore, they will not switch-off completely, but will rather switch-off in a timely fashion with the current falling and the voltage rising over a non-fixed time period.

This switching off process necessitates the implementation of dead time to the PWM. By switching one IGBT off and waiting a predetermined time period, before the other IGBT is switched on, the first IGBT is allowed to switch-off completely. This is not only done for the PWM but also for the zero voltage crossing of the tap voltage. Changing from the one IGBT pair that is switched on permanently to the other without dead time raises the possibility of short-circuiting the autotransformer taps. Using dead time during the zero voltage crossover prevents this from happening by switching off the first IGBT pair and then waiting for the entire dead time period before switching on the other IGBT pair.

The connections of the four IGBTs T_1 to T_4, shown in Figure 2.3, form two synchronous buck converters operating separately from each other. The one synchronous buck converter consists of IGBTs T_1 and T_4, which operate during the negative cycle of the tap voltage v_t. The second synchronous buck converter, consisting of IGBTs T_2 and T_3, operates during the positive cycle tap voltage v_t. Operating these two synchronous buck converters together requires a dedicated switching scheme, which controls the switching order or commutation of the IGBTs.

The commutation determines which IGBTs must be switched on permanently or pulse width modulated, depending on whether the tap voltage v_t is in the positive half-cycle or in the negative half-cycle. Figure 2.9 shows the final implementation of the PWM together with the commutation with regard to the sign magnitude of the input voltage.

During the positive half-cycle of the tap voltage v_t, IGBTs T_1 and T_4 must be switched on permanently, while IGBTs T_2 and T_3 are pulse width modulated. The reverse is applied during the negative half-cycle of the input voltage with IGBTs T_2 and T_3 switched on permanently, while IGBTs T_1 and T_4 are pulse width modulated.

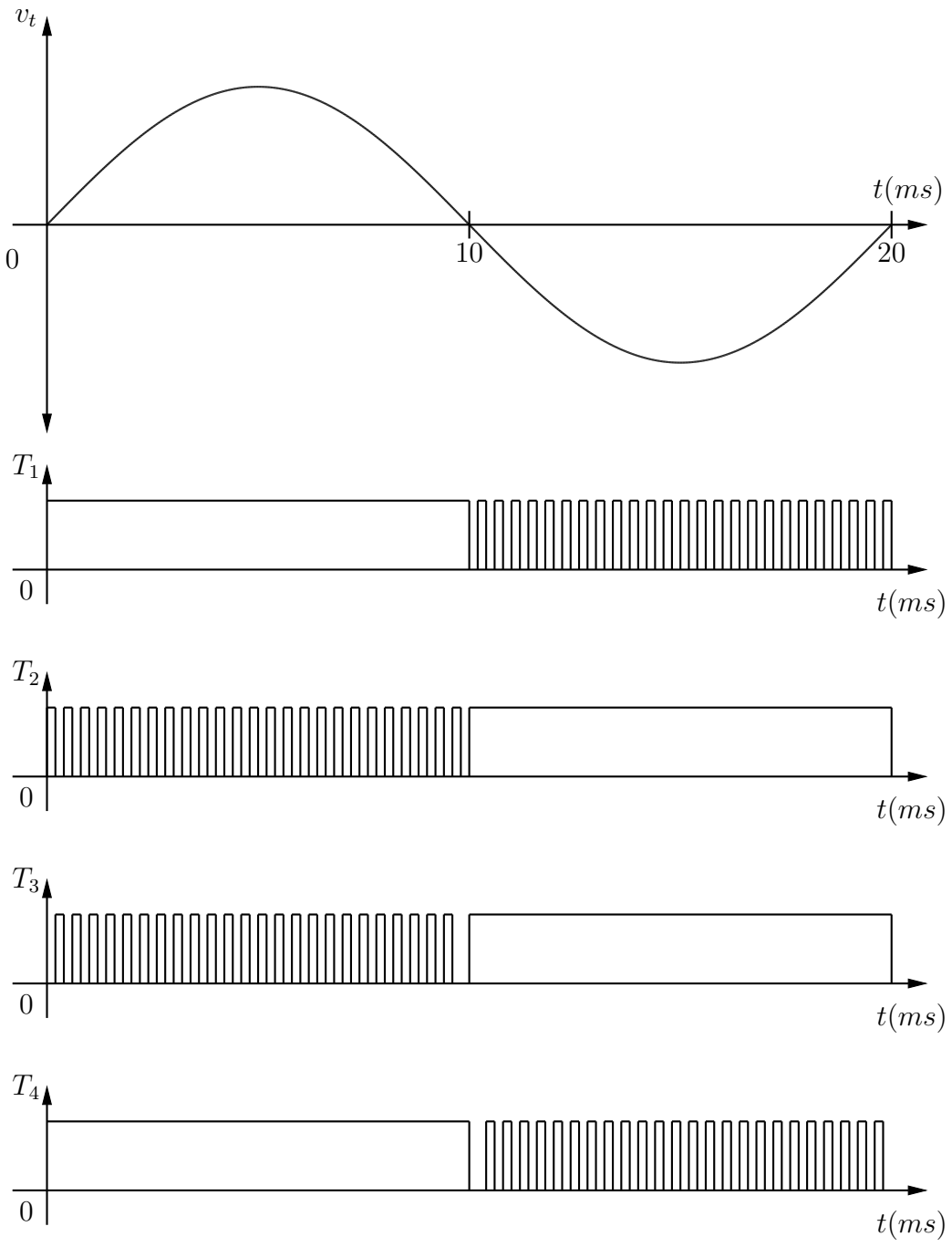

Figure 2.9: Switching scheme of the AC-chopper used in the IGBT-based tap changer.

The unfiltered result of switching the tap voltage v_t in this manner is shown in Figure 2.10 and measured at V_L which is between the connection point of IGBTs T_2 and T_3 and the output filter inductor i_L in Figure 2.3.

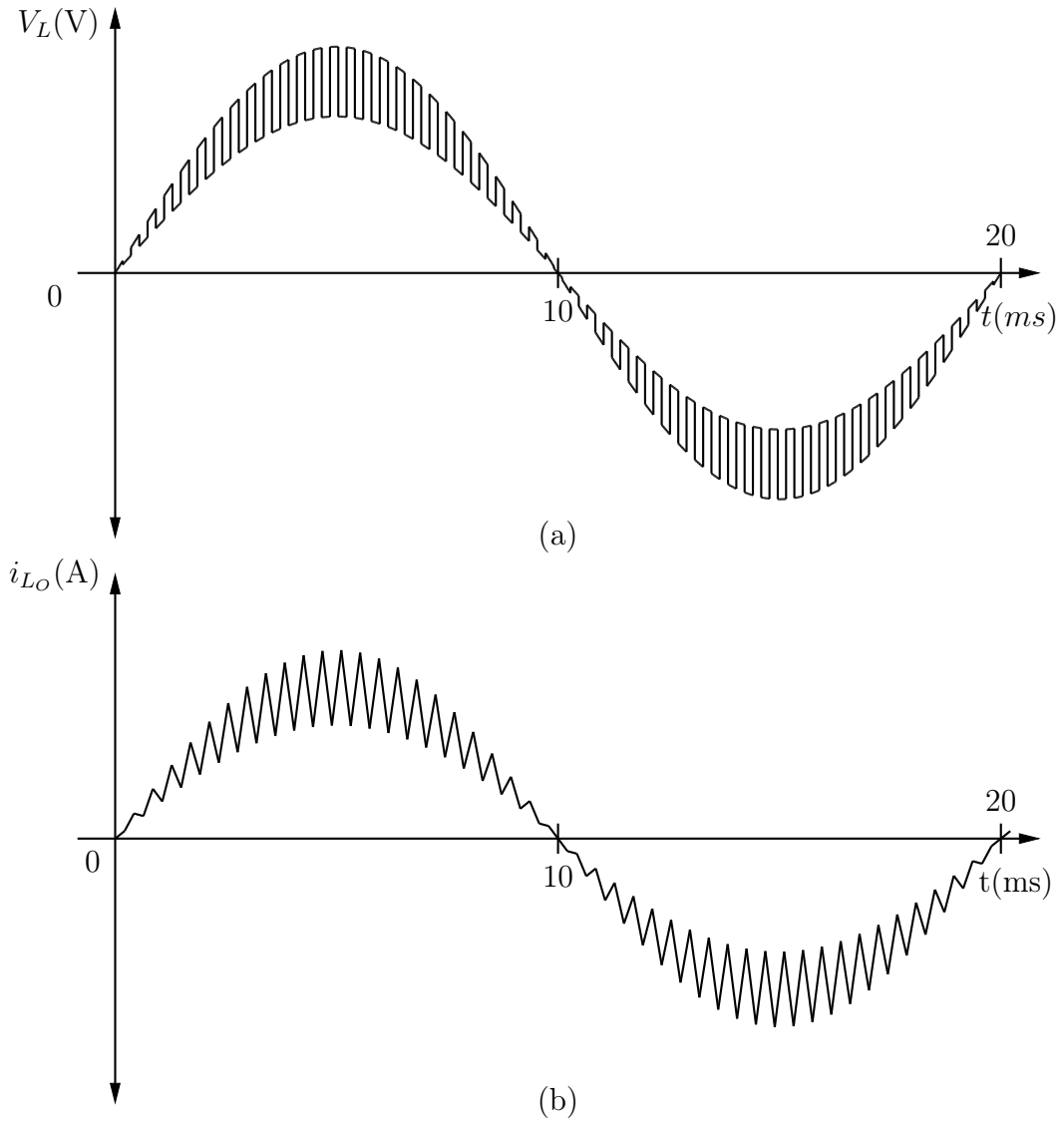

Figure 2.10: Expected unfiltered waveforms generated by the proposed switching scheme; (a) Unfiltered output voltage measured at V_L at between IGBTs T_2 and T_3; (b) Inductor current i_{L_O}.

2.4 Control method

An output feedback method is implemented to control the voltage output of the tap changer. Feeding the output voltage back into the controller allows the controller to set the duty cycle of the pulse width modulation that is used to control the IGBTs. The layout used for the feedback control method is shown below in Figure 2.11.

The following symbols are used for the controller:

- V_{ref}: Voltage reference used by the controller to determine the magnitude

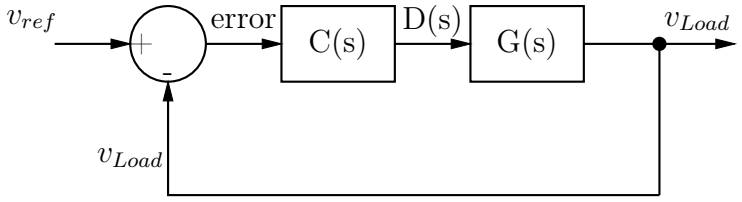

Figure 2.11: Symbolic layout of the feedback controller used in the tap changer.

of the error signal.

- error: The error signal, which is the measured load voltage V_{Load} subtracted from the reference voltage.
- C(s): The compensator, which determines the new duty cycle with regard to the error signal received.
- D(s): Duty cycle signal fed into the plant, as determined by the compensator.
- G(s): The model of the plant in a mathematical representation of the actual plant.
- V_{Load}: Load voltage.

The actual models for the plant and the compensator are evaluated in Chapter 7 for implementation in a FPGA.

2.5 Summary

This chapter presented the full system circuit diagram for the IGBT-based tap changer. The AC-chopper, which forms the converter in the IGBT-based tap changer, was discussed. The additional passive components, which filter the input and output voltages, were examined. The bypass switch that provides over-voltage and over-current protection for the IGBTs, was investigated more closely. Thereafter, the switching scheme used for the IGBTs was looked at, and the chapter ended by presenting the feedback control proposed for the IGBT-based tap changer.

Chapter 3

Detailed analysis

This chapter looks at the flow of the inductor current i_L through the IGBT-based tap changer while switching between the taps. Connecting the IGBTs between the taps, as shown in Figure 2.3, and implementing the switching scheme, set out in Figure 2.9, forces the inductor current to flow through a specific set of IGBTs and diodes. Analyzing the flow of the inductor current through the IGBTs is vital for understanding how the IGBT-based tap changer manages to regulate the load voltage.

Looking at the current flow through the IGBTs and diodes over a single period of the switching scheme provides the required insight into the operation of the IGBT-based tap changer. Analyzing the flow of the inductor current while this tap changer operates at the specifications provided in Table 3.1 provides some insight into its operation.

Description	**Symbol**	**Value**
Input voltage	v_s	6 351 V
Peak input voltage	$v_{s_{peak}}$	8 981 V
Output current	i_O	100 A
Peak output current	$i_{O_{peak}}$	141 A
Switching frequency	f_s	10 kHz
Period of switching frequency	T_s	100 μs
Tap voltage	v_t	635.1 V
Peak tap voltage	$v_{t_{peak}}$	898.1 V

Table 3.1: Operating specifications for IGBT-based tap changer.

The state of operation during which the analysis is conducted on is at the peak of the tap voltage as indicated in Figure 3.1 with the switching period indicated.

It is crucial to understand how the current flows through the IGBT-based tap changer for both positive and negative inductor current. Thus, the IGBT-

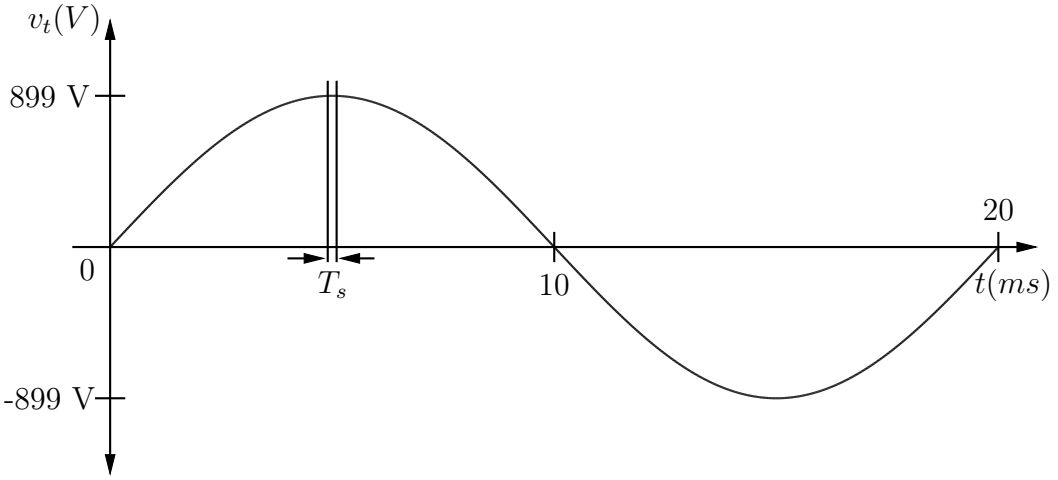

Figure 3.1: Time point at which analysis is conducted for the tap voltage v_t.

based tap changer for both currents is analysed in two separate sections. The IGBT-based tap changer during positive inductor current is analysed by using a zero degree phase shift between the tap voltage v_t and the inductor current i_L. The analysis for negative inductor current, in contrast, is done by phase shifting the tap voltage with 60° in respect of the inductor current while performing the analysis for positive tap voltage v_t.

Performing both of these analyses illustrates the independence of the current path with respect to the tap voltage.

The following section looks at the flow of the inductor current through the IGBT-based tap changer in the case of positive inductor current.

3.1 Analysis for positive inductor current

The analysis of the current flow through the IGBT-based tap changer for positive inductor current is done by means of a zero phase shift between the tap voltage and the inductor current. This zero phase shift allows the analysis to be conducted at the peak of the tap voltage v_t and inductor current i_L, as shown in Figures 3.1 and 3.2. Using the inductor current as a pure sinusoid furthermore simplifies the analysis by excluding the ripple component of the inductor current, and it also allows the peak value of the inductor current to equal the peak value of the output current i_O.

The switching period of 100 μs, together with the relatively flat peaks of the tap voltage and the inductor current, allows the analysis to be conducted on constant voltages and currents. Figure 3.3 shows the voltages over and the currents through each of the IGBTs and the anti-parallel diodes.

The diagram shows the gating signals applied to the IGBTs. The implementation of the switching scheme is evident with IGBTs T_1 and T_4 switched

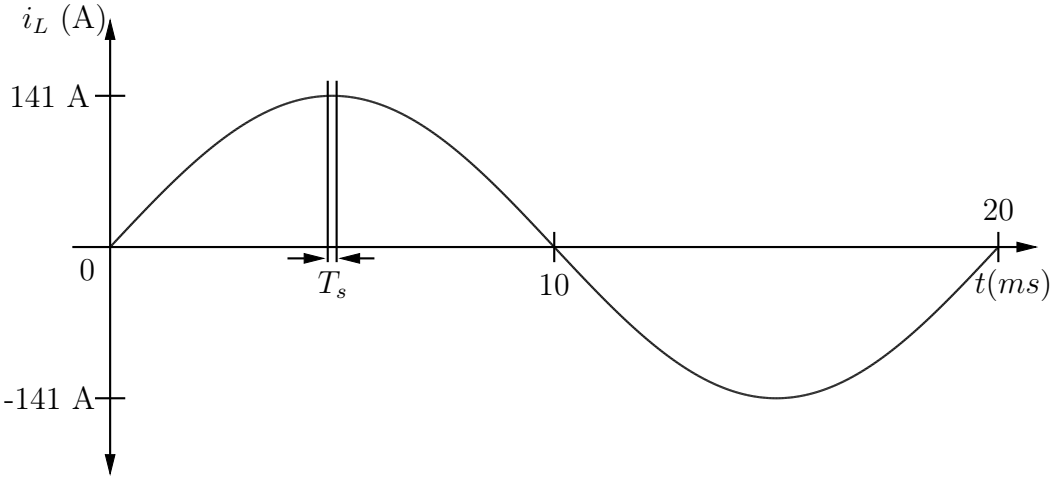

Figure 3.2: Time point at which analysis is conducted for the output current i_L.

on permanently, while T_2 and T_3 are pulse width modulated. The duty cycle of the PWM is set at 50 % including dead time.

The analysis starts at the beginning of the switching cycle with both IGBTs T_2 and T_3 switched off for the entire duration of t_1. For the duration of t_1 everything is constant, with the inductor current flowing through IGBT T_4 and diode D_3 as indicated in Figure 3.4.(c).

The IGBT-based tap changer enters t_2 in Figure 3.1 as soon as the dead time has elapsed and IGBT T_2 is switched on. The switching on process of IGBT T_2 then starts with IGBT T_2 taking over the inductor current conducted by diode D_3. During the current takeover from diode D_3 to IGBT T_2, the current i_{D_3} fall rate through the diode will equal the current $i_{c_{T_2}}$ rise rate of IGBT T_2. The path of the inductor current that occurs as a result of this exchange is shown in Figure 3.4.(b) with IGBTs T_2 and T_4 and diodes D_1 and D_3 conducting the inductor current.

The IGBT-based tap changer enters t_3 after the current has reached zero, thereby allowing diode D_3 to switch off and become reverse biased. The reverse biasing of diode D_3 allows IGBT T_2 to lower the $v_{ce_{T_2}}$ voltage over itself, while raising voltage $v_{ce_{T_3}}$ over IGBT T_3. The effect of this raising and lowering of the voltages over the IGBTs on diodes D_2 and D_3 is that the voltages $v_{F_{D_2}}$ and $v_{F_{D_3}}$ over the diodes are also raised and lowered, though only into negative values, as shown in Figure 3.3.

The current $i_{c_{T_2}}$ through IGBT T_2 does not change during t_3 and the current path of the inductor current i_L through the IGBT-based tap changer is shown in Figure 3.4.(a). After the collector-emitter voltage $v_{ce_{T_2}}$ of IGBT T_2 has reached the IGBTs saturation voltage, the IGBT-based tap changer will enter t_4(see Figure 3.3).

Nothing changes for the entire duration of t_4, as the full inductor current i_L flows through IGBT T_2; the collector-emitter voltage $v_{ce_{T_2}}$ of the IGBT

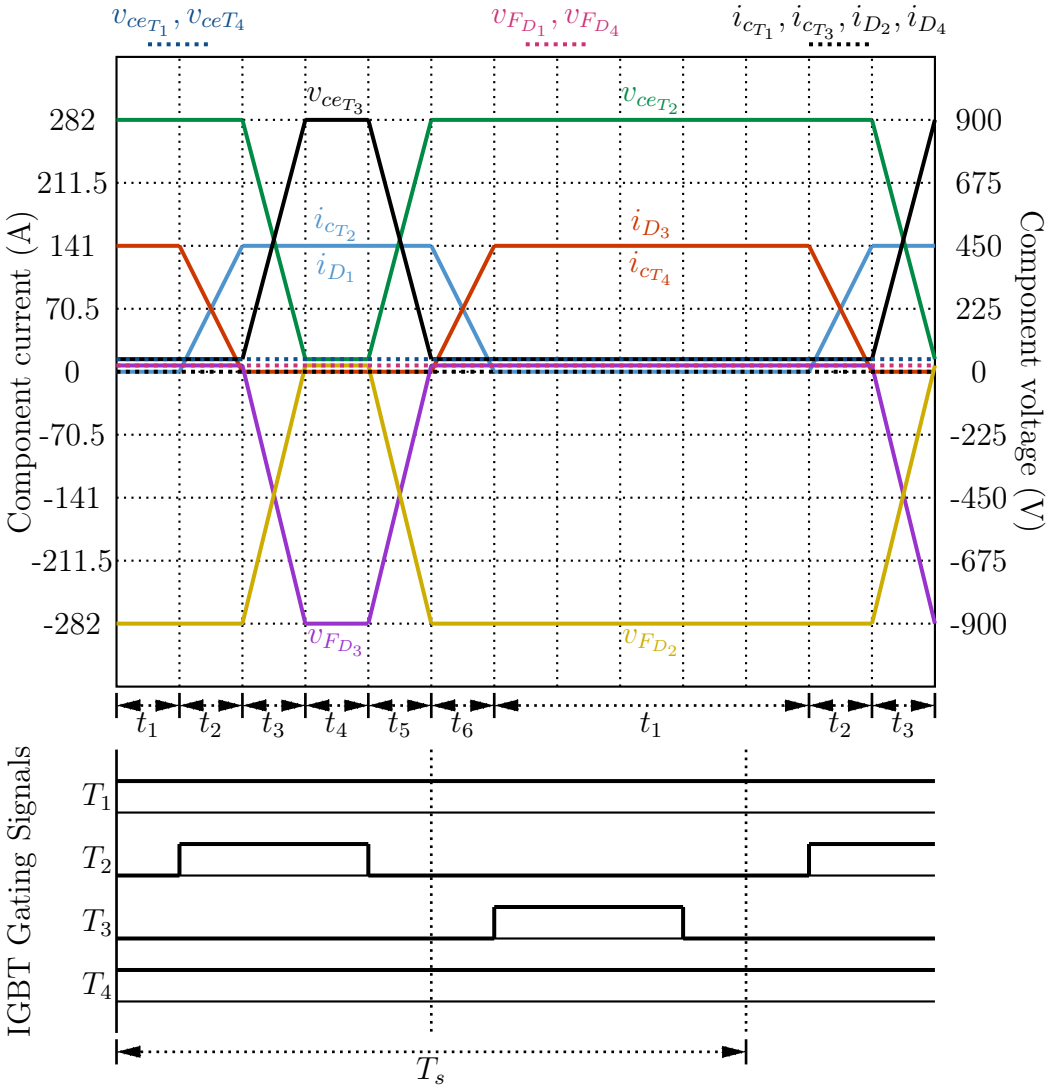

Figure 3.3: Voltage over and current through all the IGBTs and diodes together with the gating signals for the IGBTs over one switching period.

remains low, as the gating signal is applied. The time duration of t_4 depends on the duty cycle and ends before the set time of the duty cycle in order to implement the dead time.

Switching IGBT T_2 off at the end of t_4 forces the IGBT-based tap changer to enter t_5 with IGBT T_2 switching off. The switch-off process operates in reverse as the switch-on process by first raising the collector-emitter voltage $v_{ce_{T_2}}$ of IGBT T_2. This results in the $v_{F_{D_2}}$ voltage of diode D_2 becoming negative and rising negatively at the same rate as for IGBT T_2. The $v_{ce_{T_3}}$ voltage over IGBT T_3 and the $v_{F_{D_3}}$ voltage over diode D_3 decreases at the same rate as the $v_{ce_{T_2}}$ voltage over IGBT T_2 increases. The $i_{c_{T_2}}$ current flowing through IGBT T_2 does not change for the entire duration of t_5 because no other current path is

available, and it thus follows the route shown in Figure 3.4.(a). At the instant when the $v_{ce_{T_2}}$ voltage reaches the tap voltage, diode D_3 will switch on, thus allowing it to conduct the inductor current and forcing the IGBT-based tap changer into t_6.

Entering t_6 (see Figure 3.3) allows IGBT T_2 to complete the switch-off process by handing over the inductor current to diode D_3. The inductor current exchange between IGBT T_2 and diode D_3 occurs in a near linear fashion, with the rise rate of the diode current i_{D_3} equalling the current fall rate of the IGBT $i_{c_{T_2}}$. IGBT T_2 switches off completely once the current through the IGBT has reached zero.

The IGBT-based tap changer continues into t_1 after t_6 has been completed, which causes the entire process from t_1 to t_6 to repeat itself for the next switching cycle.

If a phase shift occurs between the tap voltage and the inductor current, and

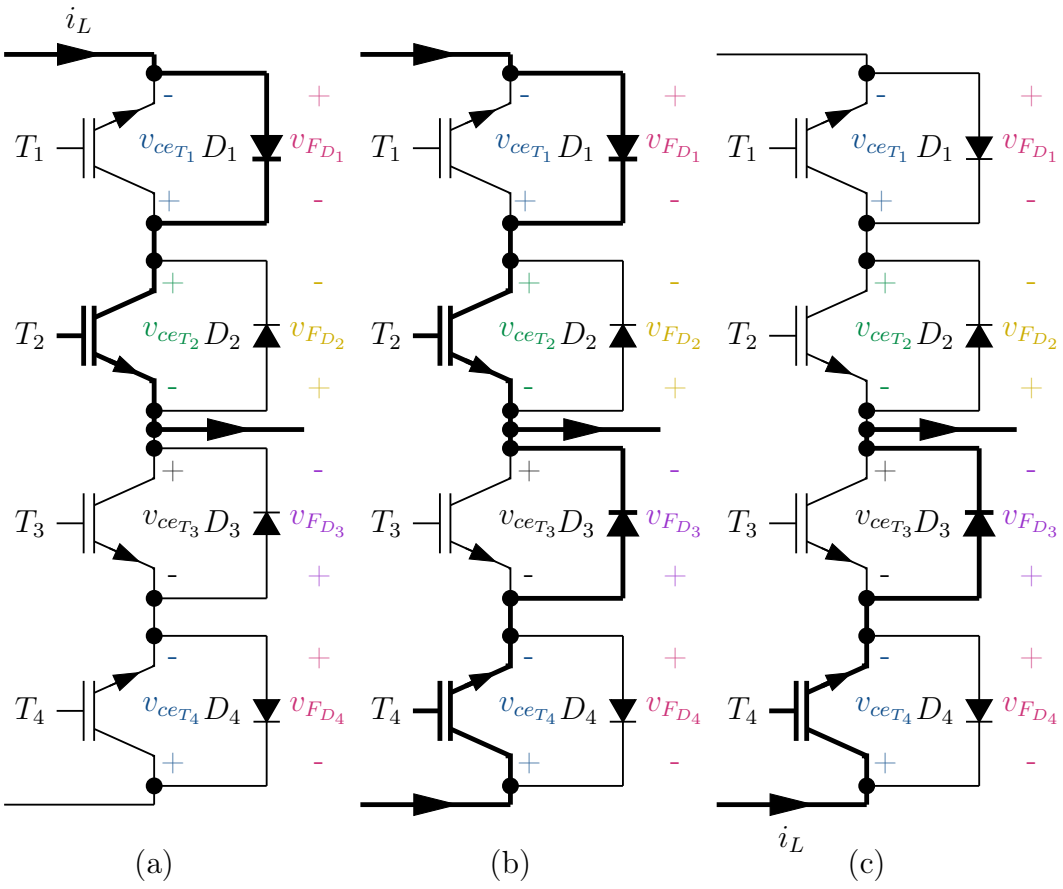

Figure 3.4: Diagrams showing the flow of positive inductor current through the IGBT-based tap changer; (a) T_2 switched on with T_2 and D_1 conducting the inductor current; (b) Both T_2 and T_3 switched off with inductor current split between T_2, T_4, D_1 and D_3; (c) T_3 switched on with T_4 and D_3 conducting the inductor current.

the inductor current thus goes negative while the tap voltage is still positive, the inductor current will simply just take a different path through the IGBT-based tap changer. This path is explained in the next section. The switchover from positive to negative inductor occurs by itself due to the bi-directional switching behaviour of the IGBTs and the anti-parallel diodes.

3.2 Negative inductor current

In this section, the flow of the inductor current through the IGBT-based tap changer while the inductor current is negative is analysed. Introducing a 60° phase shift between the tap voltage and the inductor current with the current leading provides the required situation for this analysis. Figure 3.5 shows where the analysis is conducted with regard to the phase shift between the tap voltage and the inductor current.

The analysis is performed over one switching period (namely T_s) of the switching cycle, at the position shown in Figure 3.5 with positive tap voltage while the inductor current is negative. Due to the short time duration of a single switching cycle, the magnitudes of the tap voltage and the inductor current are kept constant for the entire duration of the analysis. This helps to simplify the waveforms, which are illustrated in Figure 3.6. Excluding the ripple component of the inductor current helps to simplify the waveforms further. Using 450 V as the tap voltage at the time point relevant for the analysis and an inductor current of 70.5 A, lowers the values of the waveforms compared with Figure 3.3.

The analysis of the current flowing through the IGBT-based tap changer for negative inductor current starts at t_1. With IGBTs T_1 and T_4 switched on due to the switching scheme, and IGBT T_2 and T_3 switched off, the inductor current flows through IGBT T_1 and diode D_2, as shown in Figure 3.7.(a).

Switching on IGBT T_2 after the dead time has passed does not influence the current flowing through the IGBT-based tap changer, as the inductor current is already flowing through diode D_2. Switching IGBT T_2 on, however, provides an alternative path for the inductor current to flow in the event that the inductor current changes from negative to positive. Switching off IGBT T_2 does not influence the flow of the negative inductor current through the IGBT-based tap changer, because of the current already flowing through diode D_2.

However, if the inductor current changes from negative to positive current while IGBT T_2 is switched off, the current will flow through the snubber capacitor C_s. This situation is described in Chapter 4, when the design of the snubber capacitor is presented.

Switching on IGBT T_3 after the dead time has elapsed between IGBT T_2 and T_3 forces the IGBT-based tap changer to enter into t_2. Starting t_2 with diode D_2 conducting the full inductor current sees the current falling over time. Current i_{D_2} decreasing through diode D_2 results in current $i_{c_{T_3}}$ rising at the

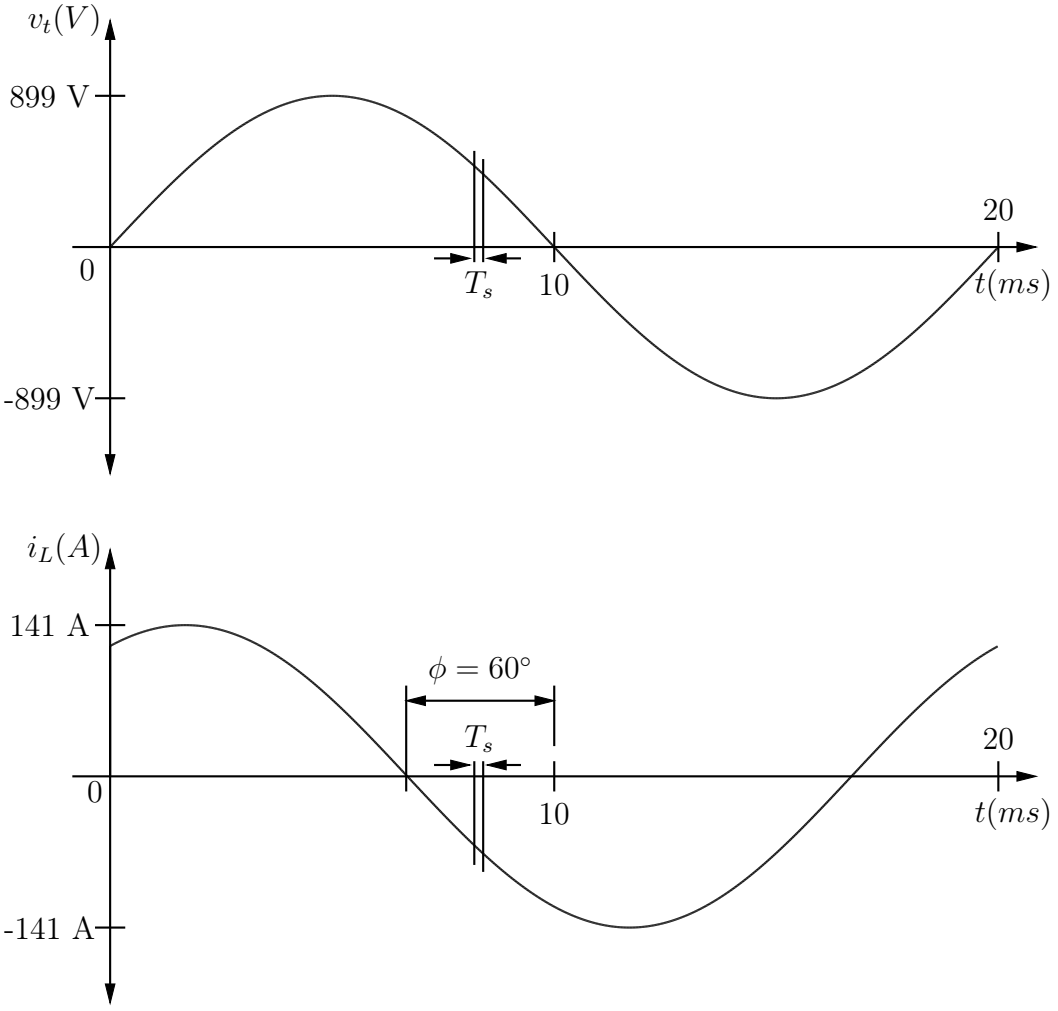

Figure 3.5: Time point at which analysis is conducted for the tap voltage v_t and output current i_L.

same rate. The handover of the current from diode D_2 to IGBT T_3 results in the inductor current flowing through both the top and bottom taps as, shown in Figure 3.7.(b).

Diode D_2 switches off after the current through the diode has reached zero, thus forcing the IGBT-based tap changer into t_3, with IGBT T_3 conducting the full inductor current, as shown in Figure 3.7.(c). The $v_{ce_{T_2}}$ voltage over the collector-emitter terminals of IGBT T_2 increases together with the $v_{F_{D_2}}$ voltage over diode D_2. The increasing voltages over IGBT T_2 and diode D_2 result in both the collector-emitter voltage $v_{ce_{T_3}}$ of IGBT T_3 and voltage $v_{F_{D_3}}$ over diode D_2 falling at the same rate and thus ending t_3. With the full tap voltage v_t over IGBT T_2 and diode D_2, while IGBT T_3 has reached full saturation voltage together with diode D_3, which has switched on completely. Once IGBT T_3 has switched on completely, together with diode D_3, while

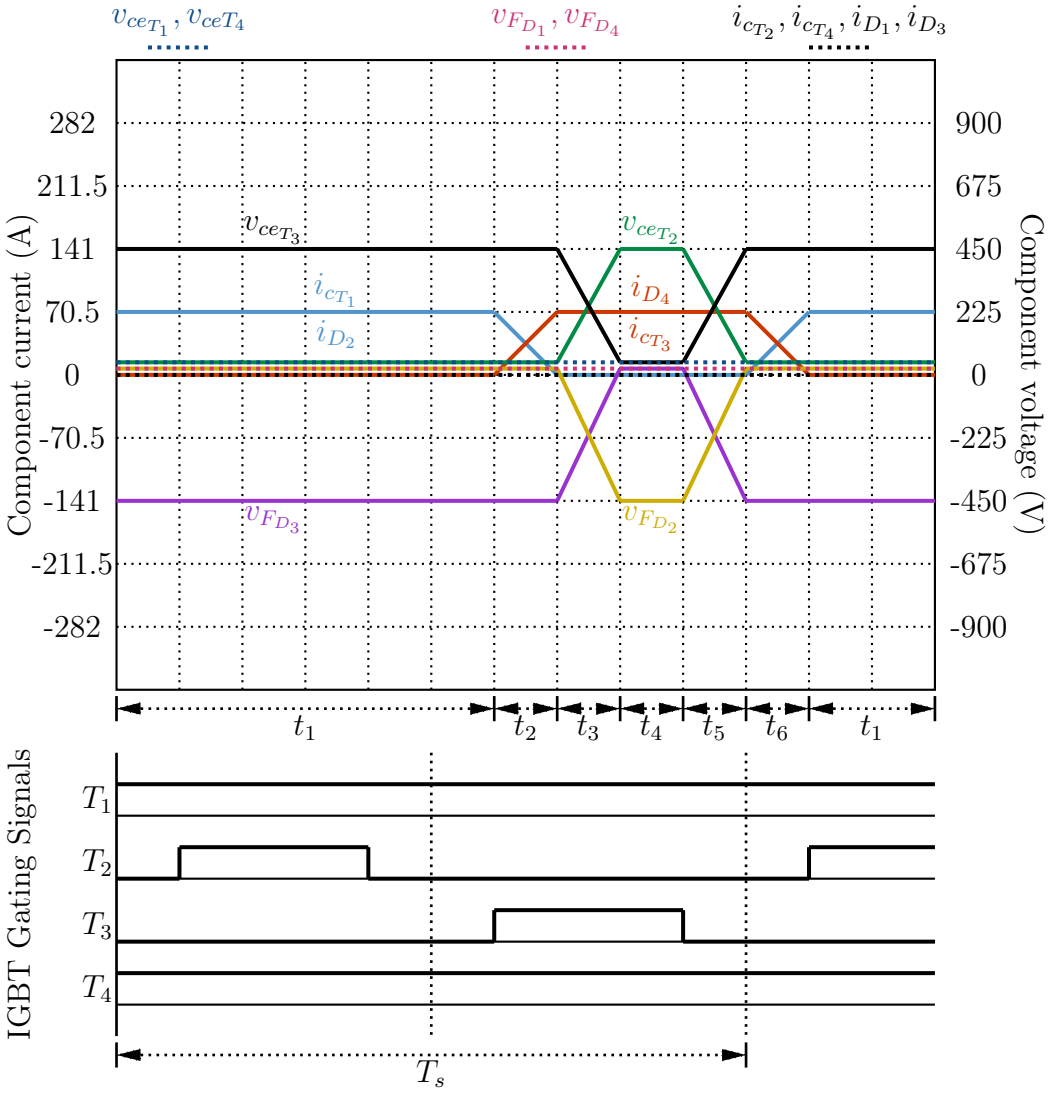

Figure 3.6: Voltage over and current through all the IGBTs and diodes together with the gating signals for the IGBTs over one switching period.

conducting the full inductor current through IGBT T_3 and diode D_4, allows the IGBT-based tap changer to enter t_4.

As nothing changes, or switches on or off for the entire duration of t_4, causes the IGBT-based tap changer operates in a steady state. The duration of t_4 is determined by the duty cycle of the PWM. It ends by switching IGBT T_3 off as determined by the duty cycle, thus resulting in the IGBT-based tap changer entering t_5. IGBT T_3 switches off by increasing the $v_{ce_{T_3}}$ voltage over its collector-emitter terminals. This, in turn, results in the $v_{F_{D_3}}$ voltage increase over diode D_3, while the voltages over IGBT T_2 and diode D_2 decreases at the same rate. t_5 ends with diode D_2 switching on after the voltage over IGBT T_3 has reached the tap voltage v_t which allows diode D_2 to take over the current

from IGBT T_3 which now enters the IGBT-based tap changer into t_6.

When diode D_2 switches on at the beginning of t_6, it allows the diode to take over the current from IGBT T_3. The rate at which IGBT current $i_{c_{T_3}}$ decreases through IGBT T_3 equals the rate at which diode current i_{D_2} increases, until diode D_2 conducts the full inductor current and IGBT T_3 switched off completely. The IGBT-based tap changer returns to t_1, with diode D_2 and IGBT T_1 conducting the full inductor current while IGBT T_3 and T_2 are both switched off. However, IGBT T_2 is switched after the dead time period has elapsed, thus providing an alternative current path if the inductor current changes from negative to positive.

The IGBT-based tap changer repeats the processes from t_1 to t_6 for each switching cycle for negative inductor current. Figure 3.5 shows the positive tap voltage v_t together with the negative inductor current at the moment of

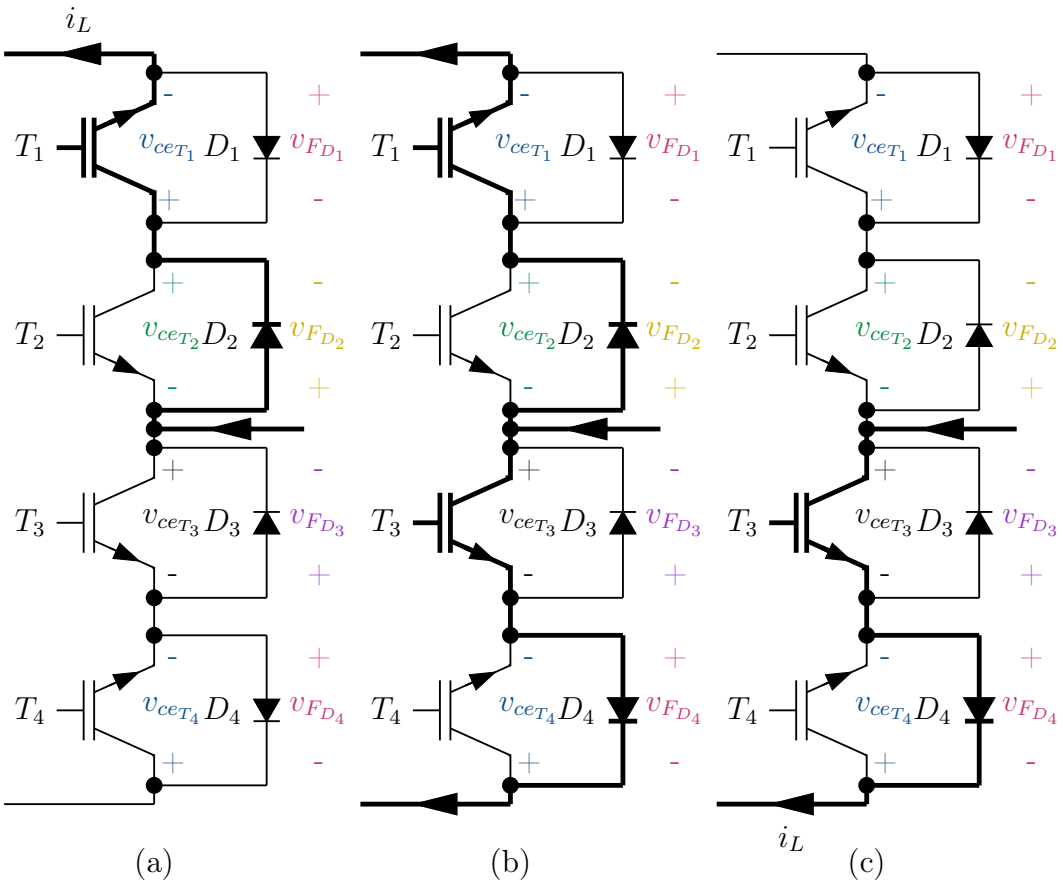

Figure 3.7: Diagrams showing negative current flowing through the IGBT-based tap changer for negative inductor current and different gating signals; (a) T_2 switched on with T_1 and D_2 conducting; (b) T_2 and T_3 switched off, with the inductor current split between top and bottom taps and flowing through T_1, T_3, D_2 and D_4; (c) T_3, switched on with T_3 and D_4 conducting the negative inductor current.

analysis. However, the tap voltage goes negative after 10 ms, while the inductor current remains negative. The only influence that the change of polarity of the tap voltage has on the IGBT-based tap changer is that is changes the switching order of the IGBTs according to the switching scheme in Figure 2.9. The current path, however, does not change as the switching order changes for the negative tap voltage change, which results in the IGBT-based tap changer switching the current through the same paths as just described.

3.3 Summary

This chapter looked at the flow of the inductor current through the IGBTs, which are used in the IGBT-based tap changer. Diagrams were to illustrate the rise and fall of all the voltages and currents in the various IGBTs and diodes. Lastly, the flow of the inductor current was analysed for both positive and negative inductor current while maintaining a positive tap voltage.

Chapter 4

Detailed design of the main components

This chapter looks in detail at the main components used in the IGBT-based tap changer. The various components covered in this chapter are listed below together with a brief description of each.

- Conduction losses: Mathematical models are derived for the conduction losses in the IGBTs and the diodes.
- Switching losses: Mathematical models are derived for the switching losses generated by the IGBTs.
- Heat sink design: A detailed heat sink analysis is done to determine the appropriate operating parameters.
- Filter components design: The circuit of the filter is simplified in order to derive a mathematical model that can be used to determine the required values for the capacitors and inductor.
- Snubber capacitor design: Mathematical equations are derived in order to calculate the required capacitance of the snubber capacitor.

4.1 Conduction losses

The losses generated in the semiconductors, which are used in the IGBT-based tap changer, consist of two components. The IGBTs generate conduction and switching losses, whereas the diodes only generate conduction losses. These losses are in the form of heat, which must be conducted away from the semiconductors to prevent them from being damaged. The design of the heat sink is explained in a following section (Section 4.3).

This section looks only at the conduction losses generated by both the IGBTs and the diodes. Conduction losses are generated while the semiconductor

is conducting the inductor current. The magnitude of these losses depends on the magnitude of the inductor current as well as the on-state voltage of the specific semiconductor.

Figure 2.3 in Chapter 2 sets out the reference position for the voltages and currents that are used to derive the equations for the conduction losses. Figure 4.1 illustrats the voltage and current waveforms through each of the semiconductors. Figure 4.1.(a) shows the tap voltage v_t over the IGBTs with a peak voltage V_T. Figure 4.1.(b) shows the inductor current i_L through inductor L_O with a peak current value I_O. The phase shift ϕ refers to the phase shift between the tap voltage v_t and the inductor current i_L with the inductor current lagging the voltage. Figures 4.1.(c) to 4.1.(f) shows the current through each IGBT and diode.

The average current [4] through the top switches T_1 and T_2 and diodes D_1 and D_2 is given by (4.1.1) below, with D referring to the duty cycle of the PWM:

$$\begin{aligned} I_{TOP} &= \frac{1}{2\pi}\int_0^{\pi} DI_O \sin\theta d\theta \\ &= \frac{DI_O}{\pi} \end{aligned} \tag{4.1.1}$$

The average current through the bottom switches T_3 and T_4 and diodes D_3 and D_4 is given by (4.1.2) below:

$$\begin{aligned} I_{TOP} &= \frac{1}{2\pi}\int_0^{\pi} (1-D)I_O \sin\theta d\theta \\ &= \frac{(1-D)I_O}{\pi} \end{aligned} \tag{4.1.2}$$

Multiplying the average current through the device with the on-state voltage gives the conduction losses generated by the devices.

The conduction losses for the top IGBTs T_1 and T_2 is given by (4.1.3) below, with $V_{ce_{(sat)}}$ referring to the on-state saturation voltage of the IGBTs:

$$P_{cond_{T_1}} = P_{cond_{T_2}} = \frac{V_{ce_{(sat)}} DI_O}{\pi} \tag{4.1.3}$$

The conduction losses for the bottom IGBTs T_3 and T_4 is given below in (4.1.4):

$$P_{cond_{T_3}} = P_{cond_{T_4}} = \frac{V_{ce_{(sat)}} (1-D)I_O}{\pi} \tag{4.1.4}$$

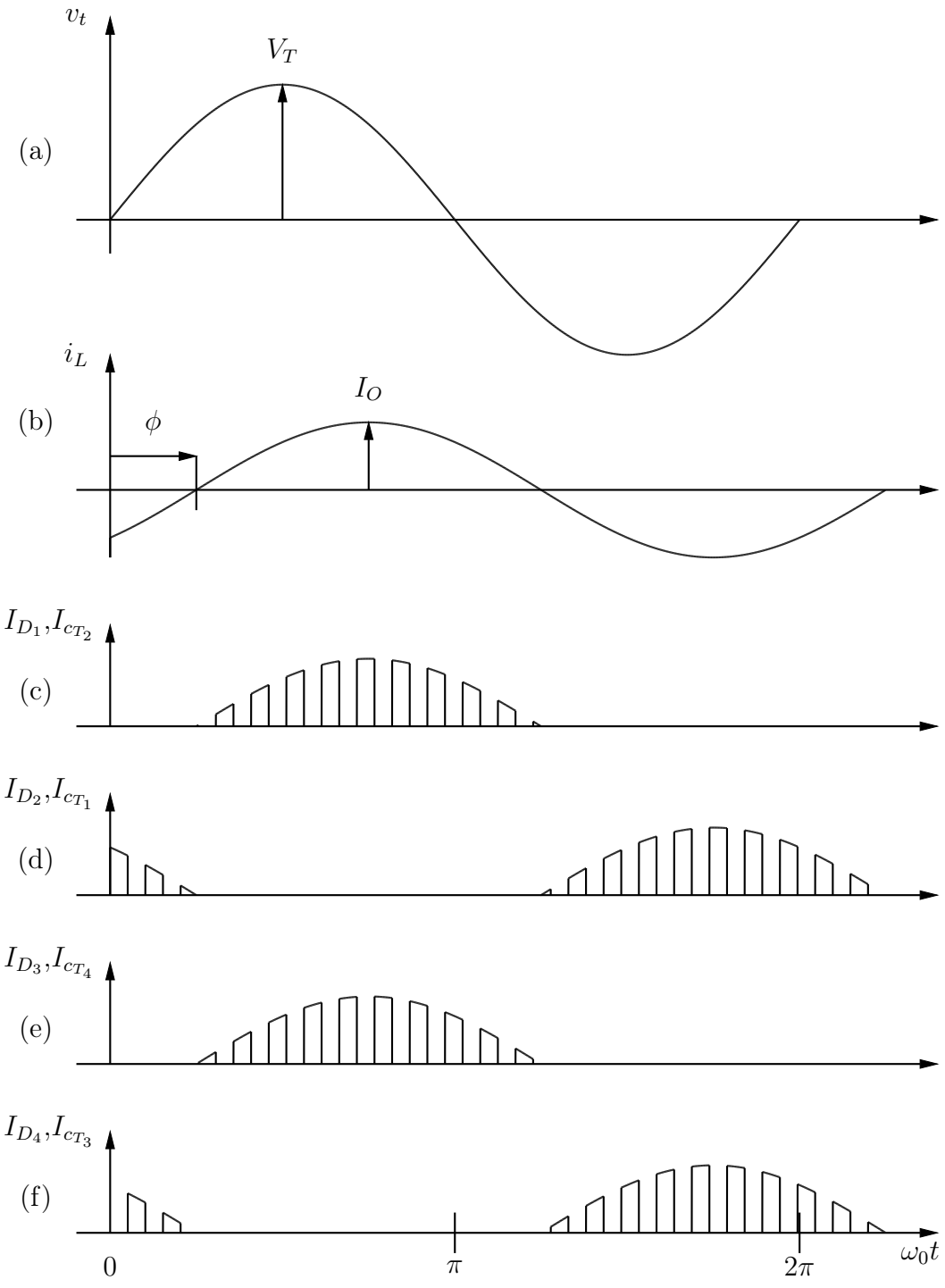

Figure 4.1: Current flowing through switches and diodes.

The conduction losses for the top diodes D_1 and D_2 is given below by (4.1.5) with V_F as the on-state forward voltage of the diode.

$$P_{cond_{D_1}} = P_{cond_{D_2}} = \frac{V_F D I_O}{\pi} \tag{4.1.5}$$

The conduction losses in the bottom diodes D_3 and D_4 expressed by (4.1.6) below:

$$P_{cond_{D_3}} = P_{cond_{D_4}} = \frac{V_F(1-D) I_O}{\pi} \tag{4.1.6}$$

The total amount of conduction losses generated is expressed by (4.1.7) below:

$$P_{cond} = 2\frac{V_{ce_{(sat)}} I_O}{\pi} + 2\frac{V_F I_O}{\pi} \tag{4.1.7}$$

4.2 Switching losses

The switching losses generated by the IGBTs represent the second component of the two loss components generated by the IGBTs, with conduction losses making up the first component. The IGBTs are the only components capable of generating switching losses, and thus this section focuses only on the IGBTs when calculating the switching losses. These are generated in IGBTs because these components dissipate energy whenever they switch-on or -off. As a result, the calculations need only focus on ascertaining the energy dissipated at those times.

Figure 4.2.a shows the tap voltage v_t and the filter inductor current i_L that are used in the switching loss calculations.

Figure 4.2 provides the basis from which the switching losses for each individual IGBT can be calculated. The equations for the switching losses for each IGBT are derived in the following sections.

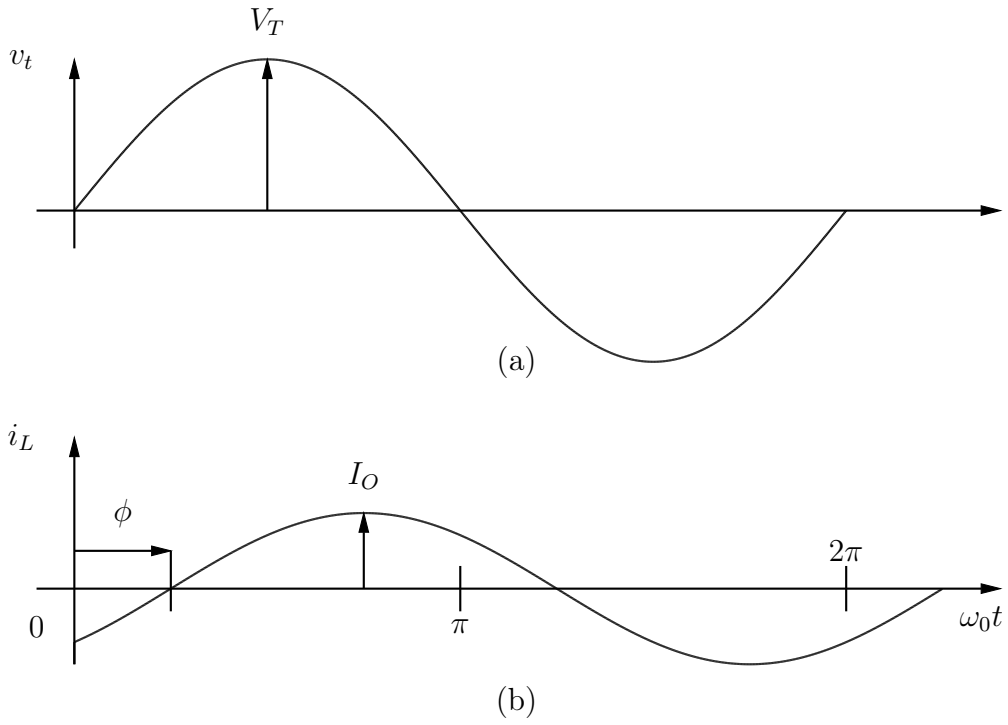

Figure 4.2: Voltage over and current through the IGBTs while switching at rated power.

4.2.1 Switching losses for IGBT T_1

The voltage over the collector-emitter terminals or V_{ce_1} voltage, as well as the collector current i_{c_1} for IGBT T_1 is depicted in Figure 4.3.

Figure 4.3 shows that the switching scheme only operates IGBT T_1 during the negative half cycle of the tap voltage v_t. The IGBT has a low switched on collector-emitter voltage, while the inductor current is flowing through the IGBTs. The IGBT conducts no inductor current while it is switched off and the collector-emitter voltage follows the tap voltage.

The switching losses for all the IGBTs are approximated [4] by summing the contribution of the switching pulses over one cycle of the fundamental, thus resulting in (4.2.1):

$$\begin{aligned} P_{sw} &= \frac{1}{T_O}\sum_k E v_{tk} i_{Lk} \\ &\approx \frac{V_T I_O E}{T_O T_s \omega_O}\int_{\pi+\phi}^{2\pi} \sin\theta \sin(\theta-\phi) d\theta \end{aligned} \tag{4.2.1}$$

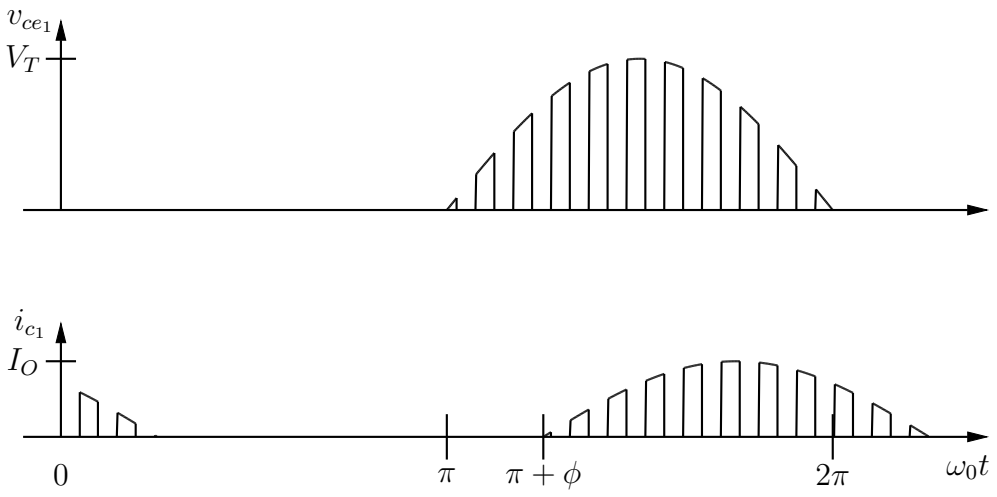

Figure 4.3: Collector-emitter voltage V_{ce_1} and collector current i_{c_1} of IGBT T_1.

With E the normalized switching energy of an IGBT given by (4.2.2) below.

$$E = \frac{E_{on} + E_{off}}{V_{CC_{test}} I_{C_{test}}} \tag{4.2.2}$$

The test voltage $V_{CC_{test}}$ and the test current $I_{CC_{test}}$ are the voltage and current at which the turn-on energy E_{on} and turn-off energy E_{off} has been measured. Dividing the turn-on and turn-off energies with the test voltage and the test current, result in the switching energy of the IGBT to be normalised.

Simplifying (4.2.1) by substituting $f_s = \frac{1}{T_s}$ and $\omega_O = \frac{2\pi}{T_O}$ into the equation results in (4.2.3) below.

$$P_{sw} = \frac{V_T I_O E f_s}{2\pi} \int_{\pi+\phi}^{2\pi} \sin\theta \sin(\theta - \phi) d\theta \tag{4.2.3}$$

Solving (4.2.3) by solving the integral part first uses (4.2.4) [12] below:

$$\sin A \sin B = \frac{1}{2}\Big[\cos(A - B) - \cos(A + B)\Big] \tag{4.2.4}$$

Substituting A = θ and B = θ - ϕ into (4.2.4):

$$\begin{aligned} \sin\theta \sin(\theta - \phi) &= \frac{1}{2}\Big[\cos(\theta - \theta + \phi) - \cos(\theta + \theta - \phi)\Big] \\ &= \frac{1}{2}\Big[\cos\phi - \cos(2\theta - \phi)\Big] \end{aligned} \tag{4.2.5}$$

Using (4.2.6) [12] to simplify the last term in (4.2.5):

$$\cos(A - B) = \cos A \cos B + \sin A \sin B \tag{4.2.6}$$

Substituting A = 2θ and B = ϕ into (4.2.6) delivers (4.2.7):

$$\cos(2\theta - \phi) = \cos 2\theta \cos\phi + \sin 2\theta \sin\phi \tag{4.2.7}$$

Substituting (4.2.7) into (4.2.5) delivers (4.2.8):

$$\sin\theta \sin(\theta - \phi) = \frac{1}{2}\cos\theta - \frac{1}{2}\cos 2\theta \cos\phi - \frac{1}{2}\sin 2\theta \sin\phi \tag{4.2.8}$$

(4.2.8) is used to solve the integral part of (4.2.3). Using ω_1 as the bottom boundary and ω_2 as the top boundary for the integral allows (4.2.9) to be used for the switching loss calculations of the other IGBTs as well.

$$\begin{aligned}
&\int_{\omega_1}^{\omega_2} \sin\theta \sin(\theta - \phi) d\theta = \int_{\omega_1}^{\omega_2} \left(\frac{1}{2}\cos\phi - \frac{1}{2}\cos 2\theta \cos\phi - \frac{1}{2}\sin 2\theta \sin\phi\right) d\theta \\
= \;& \frac{1}{2}\cos\phi(\theta)\Big|_{\omega_1}^{\omega_2} - \frac{1}{2}\cos\phi\left[\frac{1}{2}\sin 2\theta\right]\Big|_{\omega_1}^{\omega_2} + \frac{1}{2}\sin\phi\left[\frac{1}{2}\cos 2\theta\right]\Big|_{\omega_1}^{\omega_2} \\
= \;& \frac{1}{2}[\omega_2 - \omega_1]\cos\phi - \frac{1}{4}\cos\phi[\sin 2\omega_2 - \sin 2\omega_1] + \frac{1}{4}\sin\phi[\cos 2\omega_2 - \cos 2\omega_1]
\end{aligned} \tag{4.2.9}$$

(4.2.3) and (4.2.9), in conjunction with Figure 4.3, are the basis on which the switching losses for the IGBT T_1 are calculated. Since the IGBT generates switching losses only during the negative half cycle of the tap voltage v_t and since the current is phase shifted by ϕ, this results in the switching losses to be generated from $\pi + \phi$ to 2π radians, as illustrated in Figure 4.3.

Substituting (4.2.9) into (4.2.3), and using the boundaries of $\pi + \phi$ to 2π, results in switching losses for IGBT T_1 below:

$$\begin{aligned}
&P_{sw_{T_1}} = \frac{V_T I_O E f_s}{2\pi} \int_{\pi+\phi}^{2\pi} \sin\theta \sin(\theta - \phi) d\theta \\
= \;& \frac{V_T I_O E f_s}{2\pi}\left(\frac{1}{2}[2\pi - \pi - \phi]\cos\phi - \frac{1}{4}\cos\phi[\sin 4\pi - \sin(2\pi + 2\phi)]\right. \\
& \left. + \frac{1}{4}\sin\phi[\cos 4\pi - \cos(2\pi - 2\phi)]\right) \\
= \;& \frac{V_T I_O E f_s}{2\pi}\left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}\cos\phi\sin 2\phi - \frac{1}{4}\sin\phi\cos 2\phi + \frac{1}{4}\sin\phi\right) \\
= \;& \frac{V_T I_O E f_s}{2\pi}\left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}[\sin 2\phi\cos\phi - \cos 2\phi\sin\phi] + \frac{1}{4}\sin\phi\right) \\
= \;& \frac{V_T I_O E f_s}{2\pi}\left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}\sin(2\phi - \phi) + \frac{1}{4}\sin\phi\right) \\
= \;& \frac{V_T I_O E f_s}{4\pi}\left([\pi - \phi]\cos\phi + \sin\phi\right)
\end{aligned} \tag{4.2.10}$$

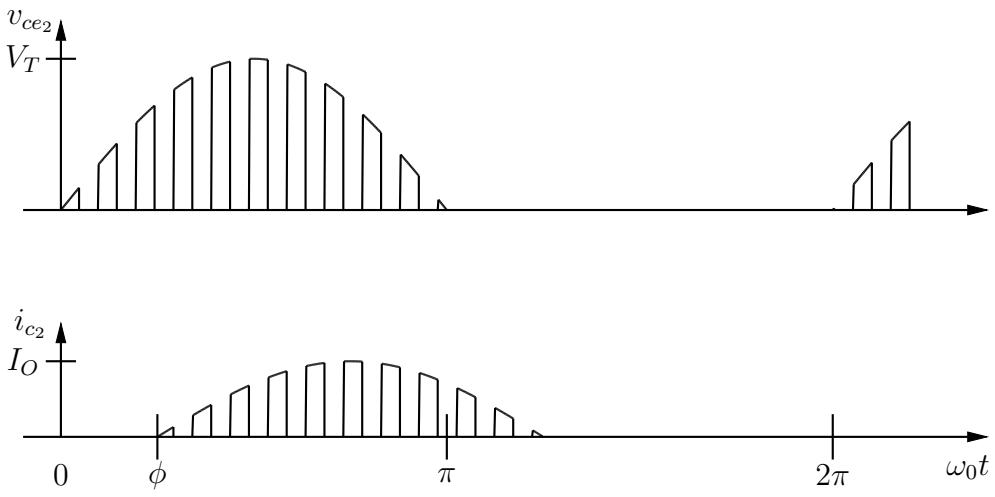

Figure 4.4: Collector-emitter voltage V_{ce_2} and collector current i_{c_2} of IGBT T_2

4.2.2 Switching losses for IGBT T_2

The switching losses for IGBT T_2 are calculated by means of the same procedure as used for IGBT T_1. The only difference is the period during which the IGBT generates the switching losses. Figure 4.4 shows the period during which the IGBT is busy switching and conducting current.

Figure 4.4 shows that IGBT T_2 is pulse width modulated during the positive cycle of the tap voltage v_t. The figure also indicates that the IGBT only conducts positive inductor current, independently of the tap voltage.

Figure 4.4 shows that IGBT T_2 is generating switching losses from ϕ to π.

Substituting (4.2.9) into (4.2.3) with the boundaries set to ϕ and π radians, results in the switching losses for IGBT T_2 as expressed by (4.2.11) below.

$$
\begin{aligned}
P_{sw_{T_2}} &= \frac{V_T I_O E f_s}{2\pi} \int_{\phi}^{\pi} \sin\theta \sin(\theta - \phi) d\theta \\
&= \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}[\pi - \phi]\cos\phi - \frac{1}{4}\cos\phi[\sin 2\pi - \sin 2\phi] \right. \\
&\quad \left. + \frac{1}{4}\sin\phi[\cos 2\pi - \cos 2\phi] \right) \\
&= \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}\cos\phi\sin 2\phi - \frac{1}{4}\sin\phi\cos 2\phi + \frac{1}{4}\sin\phi \right) \\
&= \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}[\sin 2\phi\cos\phi - \cos 2\phi\sin\phi] + \frac{1}{4}\sin\phi \right) \\
&= \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}[\pi - \phi]\cos\phi + \frac{1}{4}\sin(2\phi - \phi) + \frac{1}{4}\sin\phi \right) \\
&= \frac{V_T I_O E f_s}{4\pi} \left([\pi - \phi]\cos\phi + \sin\phi \right) \qquad (4.2.11)
\end{aligned}
$$

4.2.3 Switching losses for IGBT T_3

The switching losses generated by IGBT T_3 are calculated by means the same method as used for IGBT T_1 and T_2. Figure 4.5 shows the collector-emitter voltage $V_{ce_{T_3}}$ over the IGBT and the collector current i_{c_3} through the IGBT.

The implementation of the switching scheme is evident in Figure 4.5, and it shows that IGBT T_3 is switching during the positive cycle of the tap voltage v_t while conducting the negative inductor current i_L.

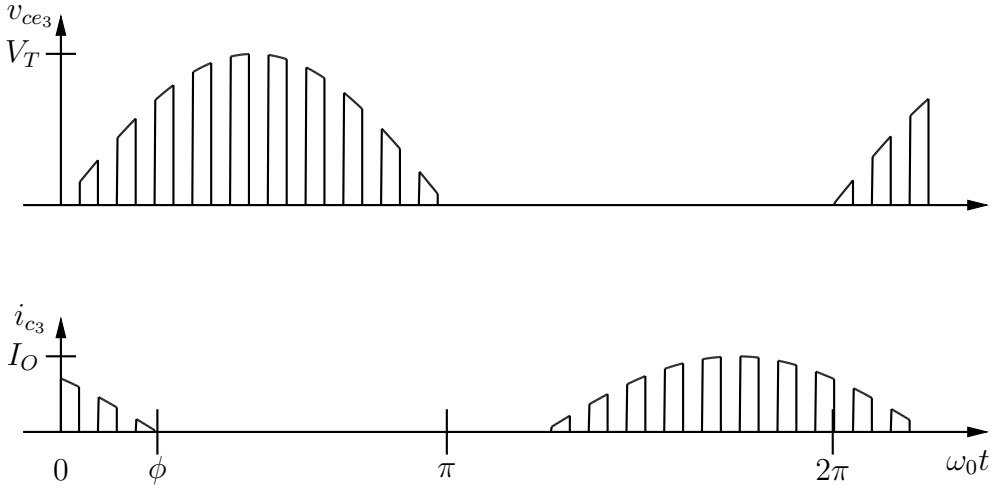

Figure 4.5: Collector-emitter voltage V_{ce_3} and collector current i_{c_3} of IGBT T_3.

IGBT T_3 generates switching losses only during the period when the tap voltage is positive and the inductor current is negative, in other word, from 0 to ϕ radians.

Substituting (4.2.9) into (4.2.3) and adding the boundaries off 0 to ϕ radians results in the switching losses for IGBT T_3 as expressed below in (4.2.12).

$$\begin{aligned}
& P_{sw_{T_3}} = \frac{V_T I_O E f_s}{2\pi} \int_0^{\phi} \sin\theta \sin(\theta - \phi) d\theta \\
= & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi\cos\phi - \frac{1}{4}\cos\phi[\sin 2\phi - \sin 0] + \frac{1}{4}\sin\phi[\cos 2\phi - \cos 0] \right) \\
= & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi\cos\phi - \frac{1}{4}\cos\phi\sin 2\phi + \frac{1}{4}\sin\phi\cos 2\phi - \frac{1}{4}\sin\phi \right) \\
= & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi\cos\phi - \frac{1}{4}[\sin 2\phi\cos\phi - \cos 2\phi\sin\phi] - \frac{1}{4}\sin\phi \right) \\
= & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi\cos\phi - \frac{1}{4}\sin(2\phi - \phi) - \frac{1}{4}\sin\phi \right) \\
= & \frac{V_T I_O E f_s}{4\pi} \left(\phi\cos\phi - \sin\phi \right) \qquad (4.2.12)
\end{aligned}$$

4.2.4 Switching losses for IGBT T_4

The same method used for calculating the switching losses for the previous IGBTs is used for IGBT T_4. Figure 4.6 shows the IGBT switching during the negative cycle of the tap voltage v_t while only conducting positive inductor current.

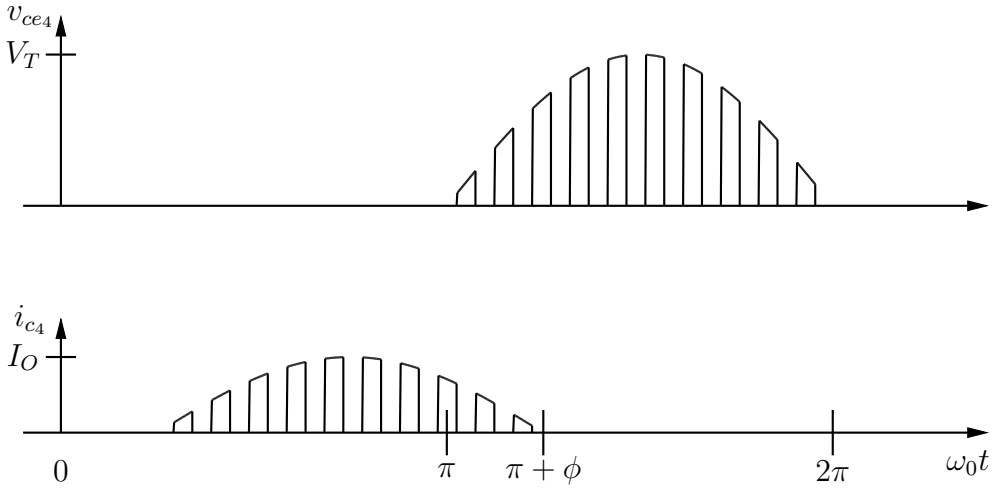

Figure 4.6: Collector-emitter voltage V_{ce_4} and collector current i_{c_4} of IGBT T_4.

The period during which IGBT T_4 generates losses is from π to $\pi + \phi$ radians as shown in Figure 4.6.

Substituting (4.2.9) into equation4.2.3 and adding the boundaries from π to $\pi + \phi$ radians delivers the switching losses for IGBT T_4 as expressed in (4.2.13) below.

$$\begin{aligned}
& P_{sw_{T_4}} = \frac{V_T I_O E f_s}{2\pi} \int_{\pi}^{\pi+\phi} \sin\theta \sin\theta - \phi d\theta \\
= \; & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}[\pi + \phi - \pi] \cos\phi - \frac{1}{4} \cos\phi [\sin(2\pi + 2\phi) - \sin 2\pi] \right. \\
& \left. + \frac{1}{4} \sin\phi [\cos(2\pi + 2\phi) - \cos 2\pi] \right) \\
= \; & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi \cos\phi - \frac{1}{4} \cos\phi \sin 2\phi + \frac{1}{4} \sin\phi \cos 2\phi - \frac{1}{4} \sin\phi \right) \\
= \; & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi \cos\phi - \frac{1}{4}[\sin 2\phi \cos\phi - \cos 2\phi \sin\phi] - \frac{1}{4} \sin\phi \right) \\
= \; & \frac{V_T I_O E f_s}{2\pi} \left(\frac{1}{2}\phi \cos\phi - \frac{1}{4} \sin(2\phi - \phi) - \frac{1}{4} \sin\phi \right) \\
= \; & \frac{V_T I_O E f_s}{4\pi} \left(\phi \cos\phi - \sin\phi \right) \qquad (4.2.13)
\end{aligned}$$

The above equations that have been derived for the switching losses for all IGBTs include the phase shift between the voltage and current. However, if the phase shift is leading, the equations will deliver a negative value. This is not possible in practice. This must therefore be accounted for when calculating the switching losses, as it can influence the results if it is ignored.

4.3 Heat sink design

The various types of losses analysed in the previous sections all create heat in the IGBTs. This heat forms at the junction of the IGBTs, and it must be conducted away from these before the junction temperature exceeds the maximum allowable junction temperature. If this happens, it may damage the IGBTs; consequently, adequate cooling must be used to cool the IGBTs.

Many different methods can be employed to cool the IGBTs, but all these methods make use of a heat sink. This provides a physical platform for the IGBTs. Essentially, it conducts the heat away from the casing of each IGBT module, causing the heat sink itself to warm up over time. The heat sink warms up until a state of equilibrium is reached between the amount of heat it absorbs and the amount of heat it dissipates. If too much heat is generated by the components and the heat sink cannot dissipate it effectively to cool the IGBTs, then additional cooling methods must be used.

One option is to use a larger heat sink, as this provides a larger contact area to the surrounding air. But there are practical limitations with this too, due to the weight and size of the heat sink. Other options involve active cooling solutions that range from forced air cooling to water cooling and oil cooling. Forced air cooling makes use of fans blowing air over the fins of the heat sink, thereby cooling it down. As this is the cheapest and easiest to install, forced air cooling is a viable choice, but it is not as effective as water or oil cooling.

Water cooling makes use of a specially designed heat sink, which allows water to flow via pipes through the core of the heat sink. But designing such a water cooling system is consequently more complicated, because it must accurately determine the pressure and volume of water that has to flow through the pipes to cool the heat sink the most effectively. The risk of water leakages in a high voltage system poses a major risk when using such a system inside the IGBT-based tap changers.

Oil cooling use more or less the same type of design as that used for water cooling, but the risk of a leak does not present such a major risk. In both cases, however, another potential problem comes from the pumps required to circulate either the oil or the water. If the pump fails, it will stop all coolant flowing between the heat sink and the cooling source; this will prevent the heat sink from cooling down, which can potentially damage the IGBTs. Using forced air cooling, in contrast, does not pose the same level of risk if the fans should fail, due to the size of the heat sink used.

In view of the above, the cooling solution that was implemented in our system included a heat sink, supplemented with fan-assisted forced air cooling. The ease of design, as well as its straightforward implementation and the lower risks meant that forced air cooling was the most sensible choice in these circumstances.

The heat sink was designed in such a way that all four IGBTs were mounted onto a single heat sink, thereby minimizing the space required for the heat sink. Figure 4.7 [4] shows the thermal model used for this particular heat sink design. The thermal design takes into account the thermal resistance of each device as a resistance, while showing the temperatures at different locations within the system.

Heat generated at the junction of IGBT T_1 raises the junction temperature $T_{j_{T_1}}$ of the IGBT. This forces heat to flow from the junction to the case of the IGBT module due to the temperature difference over the thermal resistance $R_{th_{T_1}(j-c)}$ of the IGBT. Heat flowing to the case of the IGBT module raises the case temperature $T_{c_{M_1}}$ of the module. This in turn creates a temperature difference over the thermal resistance $R_{th_{M_1}(c-s)}$ of the module, with the case temperature $T_{M_1(c-s)}$ higher than the heat sink temperature T_s. This temperature difference allows heat to flow from the case of the IGBT module to the heat sink, thus causing the heat sink temperature T_s to rise. The temperature difference over the thermal resistance of the heat sink $R_{th_{sink}(s-a)}$, with the sink temperature T_s higher than the ambient temperature T_a, allows heat to

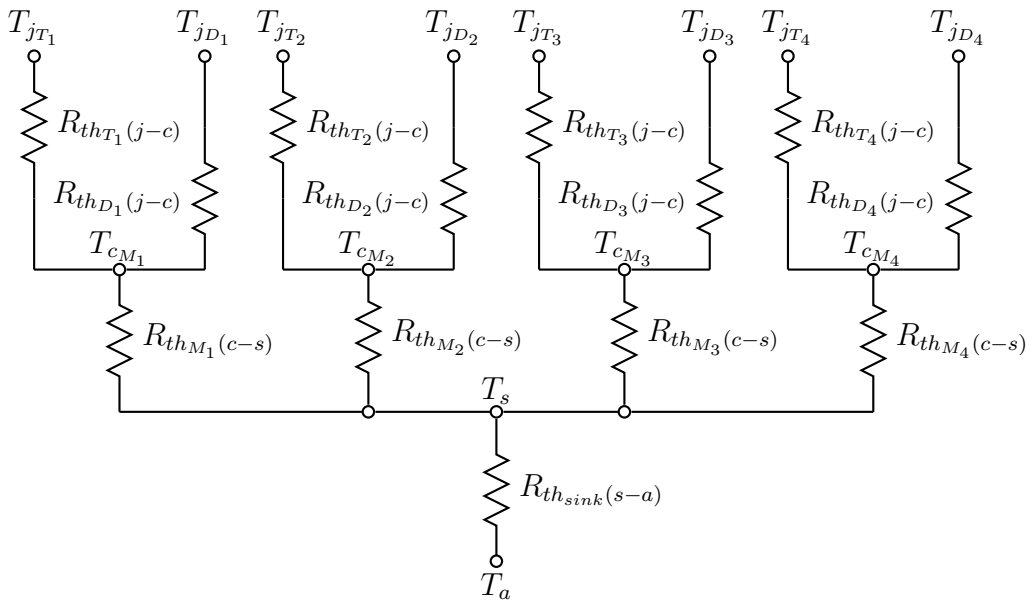

Figure 4.7: Thermal model of four IGBTs placed on one heat sink.

flow through the heat sink to the outside. The air generated by the fans and flowing over the heat sink extracts the heat, cooling the heat sink down. The heat sink also cools down through natural convection.

This flow of heat sustains itself, because the losses inside the IGBTs are continuously generating heat. The generated heat keeps the junction temperature at its highest level, which drops across the different measuring points until it reaches the ambient temperature, where it is the lowest. The same process holds for all the other IGBTs and diodes.

The first step of designing the heat sink was to choose a heat sink that would be easily obtainable and then to calculate the maximum switching frequency for that specific heat sink. The thermal model in Figure 4.7 was then simplified, and thereafter an equation was derived to provide the maximum switching frequency of the IGBT-based tap changer. This design process was implemented in Chapter 5.

The switching scheme implemented to control the IGBTs of the IGBT-based tap changer forces IGBTs T_1 and T_4 to form one switching pair and IGBTs T_2 and T_3 the other switching pair. According to the analysis conducted in Chapter 3, only one IGBT generates switching and conduction losses at any given moment, while one diode conducts the inductor current. The losses generated by the switching of an IGBT generates the largest amount of heat, resulting in the design to be done for IGBT T_1. Thus, designing the heat sink with the tap voltage negative as well as the inductor, this designs the heat sink for the losses of IGBT T_1 as well as the conduction losses of diode D_2. However, designing the heat sink for any other configuration, delivers the same results.

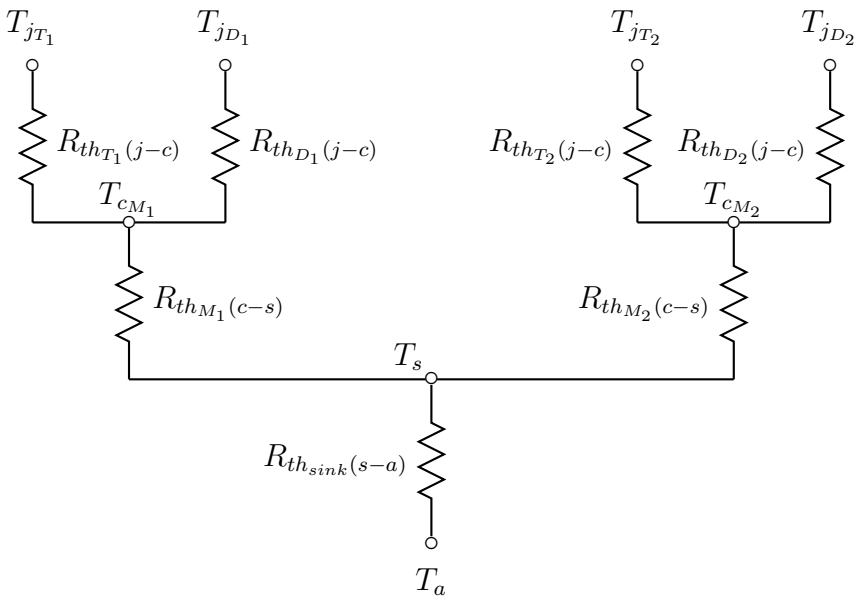

Figure 4.8: Thermal model of two IGBTs with anti-parallel diodes placed on a single heat sink.

The heat sink design is thus done by incorporating the maximum negative tap voltage over the IGBTs with a zero phase shift between the tap voltage and the load current. Implementing a zero phase shift with $\phi = 0$ into (4.2.10) and (4.2.13) results in IGBT T_1 generating all the switching losses, while IGBT T_4 generates none. This forces the heat sink design to be done with only IGBT T_1 generating switching losses, while diode D_2, generates the conduction losses. The conduction losses of diode D_4 and IGBT T_3 are thus not taken into account in the heat sink design because these components are not generating losses at the same time as the switching and conduction losses for IGBT T_1 and diode D_2. The switching losses of IGBT T_1 are also larger than the conduction losses of IGBT T_3 and diode D_4 together. As a result the heat sink design only took into account the losses of IGBT T_1 and diode D_2.

Figure 4.8 shows the thermal model for IGBT T_1 together with diode D_2.

The maximum amount of heat that can be dissipated by the heat sink in the form of power is given by (4.3.1) below.

$$P_{sink} = \frac{T_s - T_a}{R_{th_{sink}(s-a)}} \tag{4.3.1}$$

The maximum amount of heat that the heat sink can dissipate can also be calculated as the sum of the heat generated by IGBT T_1 and diode D_2 in (4.3.2) below.

$$P_{sink} = P_{D_2} + P_{T_1} \tag{4.3.2}$$

The losses generated by diode D_2 consists only of conduction losses, which are calculated with (4.1.5). The heat losses generated by IGBT T_1 are expressed in (4.3.3).

$$P_{T_1} = \frac{T_{j(max)} - T_s}{R_{th_{T_1}(j-c)} + R_{th_{M_1}(c-s)}} \tag{4.3.3}$$

Substituting (4.3.1) and (4.3.3) into (4.3.2) provides the maximum sink temperature T_s in (4.3.4) below.

$$\begin{aligned} \frac{T_s - T_a}{R_{th_{sink}(s-a)}} &= P_{D_2} + \frac{T_{j(max)} - T_s}{R_{th_{T_1}(j-c)} + R_{th_{M_1}(c-s)}} \\ T_s &= \left(P_{D_2} + \frac{T_a}{R_{th_{sink}(s-a)}} + \frac{T_{j(max)}}{R_{th_{T_1}(j-c)} + R_{th_{M_1}(c-s)}} \right) \\ &\quad \left(\frac{R_{th_{sink}(s-a)} \left[R_{th_{T_1}(j-c)} + R_{th_{M_1}(c-s)} \right]}{R_{th_{sink}(s-a)} + R_{th_{T_1}(j-c)} + R_{th_{M_1}(c-s)}} \right) \end{aligned} \tag{4.3.4}$$

The losses generated by IGBT T_1 in (4.3.5) results from calculating T_s in (4.3.4) and then substituting (4.3.1) into (4.3.2) with T_s known.

$$\begin{aligned} P_{T_1} &= P_{sink} - P_{D_2} \\ &= \frac{T_s - T_a}{R_{th_{sink}(s-a)}} - P_{D_2} \end{aligned} \tag{4.3.5}$$

But the total losses generated by the IGBT T_1 consist of both conduction and switching losses shown in (4.3.6) below.

$$P_{T_1} = P_{cond_{T_1}} + P_{sw_{T_1}} \tag{4.3.6}$$

The conduction losses $P_{cond_{T_1}}$ for IGBT T_1 are expressed (4.1.3). The switching losses $P_{sw_{T_1}}$ for IGBT T_1 are calculated by means of (4.2.10), but the phase angle $\phi = 0$ simplifies (4.2.10) into the following.

$$P_{sw_{T_1}} = \frac{V_T I_O E f_s}{4} \tag{4.3.7}$$

Solving f_s in (4.3.7) and substituting (4.3.6) into (4.3.7) results in the maximum allowable switching frequency given below in (4.3.8).

$$f_{s(max)} = \frac{4(P_{T_1} - P_{cond_{T_1}})}{V_T I_O E} \tag{4.3.8}$$

4.4 Filter components design

The filtering mechanism used for the IGBT-based tap changer consists of capacitors C_1 and C_2 together with output inductor L_O.

The components are connected as shown in Figure 4.9; this allows the capacitors C_1 and C_2 to act together as an input and output filter at the same time.

The output inductor L_O connects between the converter and the load to filter out the switching harmonics, whereas capacitors C_1 and C_2 provide a return path for the inductor ripple current.

Simplifying the layout in Figure 4.9 involves replacing the autotransformer with two ideal voltage sources v_{s_1} and v_{s_2}. L_1 represents the leakage inductance of the series winding of the autotransformer.

Current sources I_1 and I_2 in Figure 4.9 represent the current through the respective IGBTs. Current source I_1 represents the current through IGBTs T_1 and T_2 while I_2 denotes the current through IGBTs T_3 and T_4. The current waveforms of I_1 and I_2 are shown in Figure 4.11 and, when added together, signify the output current i_O.

Using superposition simplifies the filter model in Figure 4.9 by short-circuiting the voltage source v_{s_1} and v_{s_2}. The output inductor L_O is omitted because it is not relevant for the design of the capacitors. The resulting model is shown in Figure 4.10.

The simplified filter model illustrated in Figure 4.10 is in fact made up of

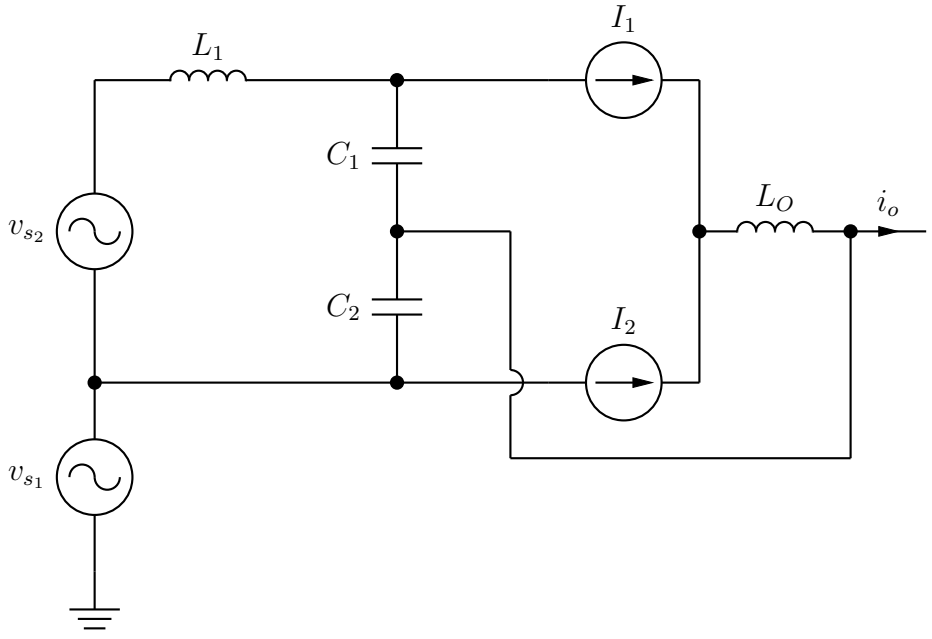

Figure 4.9: Filter components consisting of capacitors C_1 and C_2 together with inductor L_O.

two models. Figure 4.10.(a) shows current source I_1 with I_2 open circuited, while Figure 4.10.(b) shows I_2 with I_1 open circuited.

It must be noted that the models given in Figures 4.10.(a) and 4.10.(b) are symmetrical with only the current sources changing. This allows the design to be done for only one model, since the same results can be gathered with the other.

Capacitors C_1 and C_2 have been designed with respect to the model in Figure 4.10.(a). The goal of the design is to minimize the impedance in the current path for current I_a while maximizing the impedance for current path I_b. Designing the filter components in this manner limits the amount of the ripple component which goes through the series winding of the autotransformer. The current flow through I_a with respect to I_1 is summarised by (4.4.1) below.

$$I_a = \frac{sL + \frac{1}{sC}}{\frac{1}{sC} + \frac{1}{sC} + sL_1} I_1 \tag{4.4.1}$$

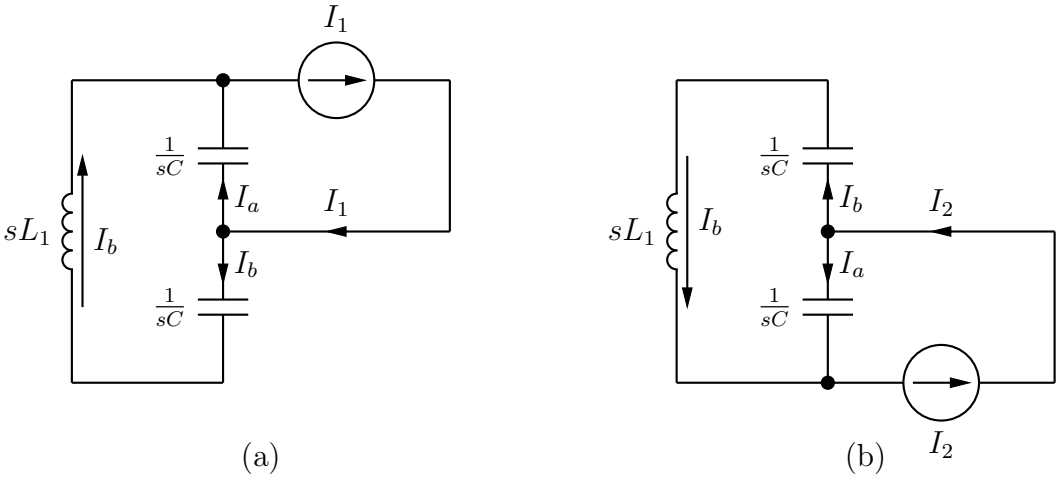

Figure 4.10: Simplified filter models; (a) Simple filter model with I_1 conducting and I_2 open circuited; (b) Simple filter model with I_2 conducting and I_1 open circuited.

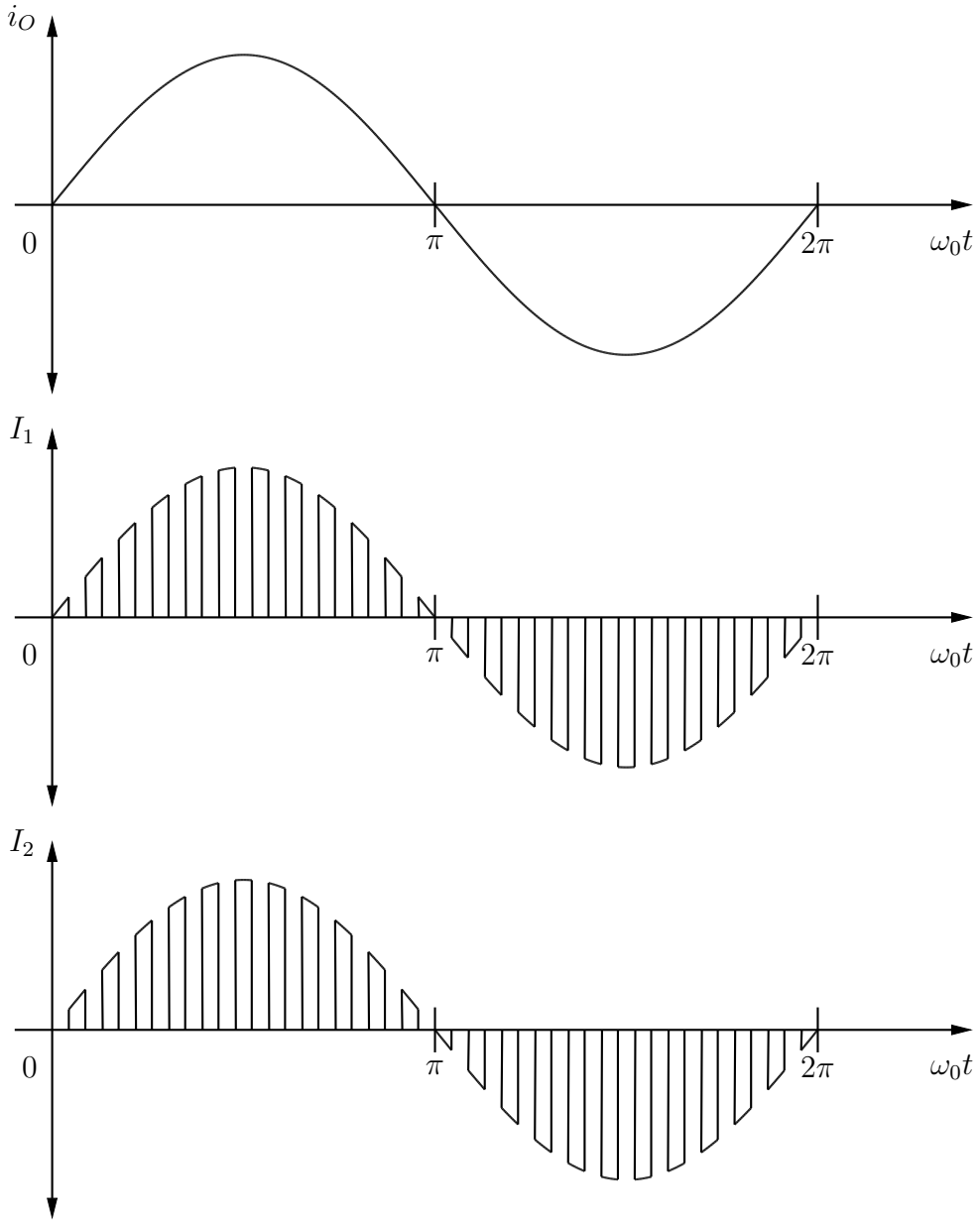

Figure 4.11: Current waveform used to represent the current source I_1 and I_2 with respect to the output current i_O.

Choosing the amount of current that flows through I_a to be 95% of I_1 results in the capacitance of C_1 and C_2, with ω the cut-off frequency of the filter:

$$\begin{aligned}
I_a &= \frac{sL_1 + \frac{1}{sC}}{\frac{1}{sC} + \frac{1}{sC} + sL_1} I_1 \\
0.95I_1 &= \frac{sL_1 + \frac{1}{sC}}{\frac{1}{sC} + \frac{1}{sC} + sL_1} I_1 \qquad (I_a = 0.95I_1) \\
0.95(\frac{2}{sC} + sL_1) &= sL_1 + \frac{1}{sC} \\
\frac{1}{sC}(1.9 - 1) &= sL_1(1 - 0.95) \\
0.9\frac{1}{sC} &= 0.05sL_1 \\
C &= \frac{0.9}{0.05s^2L_1} \\
C &= \frac{18}{\omega^2 L_1} \qquad (s = j\omega) \quad (4.4.2)
\end{aligned}$$

The inductance of inductor L_O is calculated by using the same method as that of a synchronous buck converter operating in the continuous-conduction mode, because the AC-chopper used in the IGBT-based tap changer inherently consists of two synchronous buck converters. The maximum peak-to-peak ripple current of inductor L_O is calculated by means of (4.4.3) [13] below.

$$\Delta_{i_L} = \frac{D(1-D)V_t}{L_O f_s} \tag{4.4.3}$$

Reworking (4.4.3) results in the inductance of inductor L_O to be calculated by (4.4.4) below.

$$L_O = \frac{D(1-D)V_t}{\Delta_{i_L} f_s} \tag{4.4.4}$$

4.5 Snubber capacitor design

The design of the snubber capacitor C_s depends on the operating conditions of the capacitor. The capacitor, as already stated in Chapter 2, conducts the inductor current i_L in two different situations: firstly, during the dead time of the switching scheme and, secondly, after the power to either the controller or the IGBT driver circuits has failed. The current path followed by the inductor current during either of these two situations is depicted below in Figure 4.12 for both positive and negative inductor current.

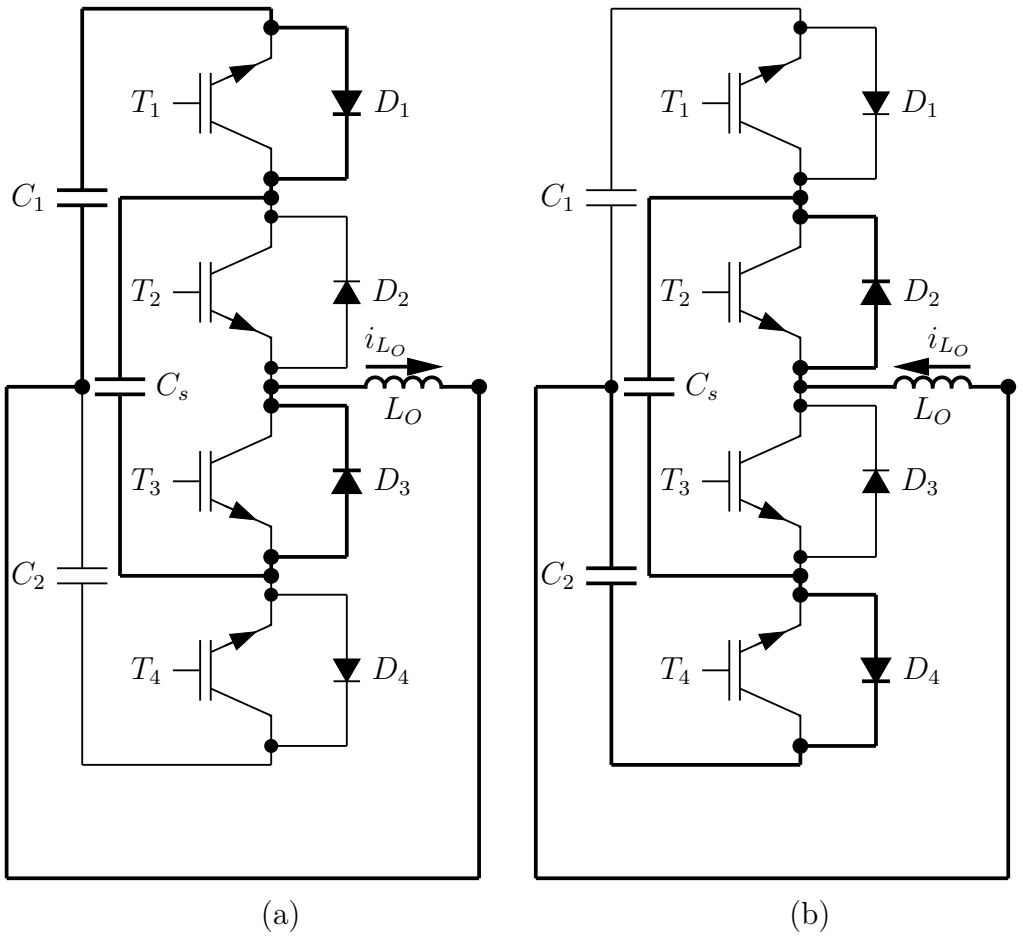

Figure 4.12: Current path of the inductor current: (a) Positive inductor current; (b) Negative inductor current.

The capacitance of the snubber capacitor is designed for the dead time period during which the snubber capacitor conducts the inductor current. It was designed in this way because it is the only situation with a constant and known time duration. However, the only time at which the snubber capacitor will be used extensively, is during the zero crossing of the tap voltage. The switching scheme thus implements dead time during the zero voltage crossings of the tap voltage in order to prevent the IGBTs from short-circuiting the transformer taps. Figure 4.13 shows the worst case scenario, which is when the snubber capacitor operates with a 30° phase shift between the tap voltage and the inductor current. The worst case scenario also assumes that the IGBTs operate as ideal switches that switch on and off immediately after the gating signals have been applied or removed respectively.

Figure 4.13 shows that the capacitor voltage increases directly after the gating signal for IGBT T_1 and T_4 has been removed at the moment, exactly when the tap voltage crosses zero. The capacitor voltage rises because it offers

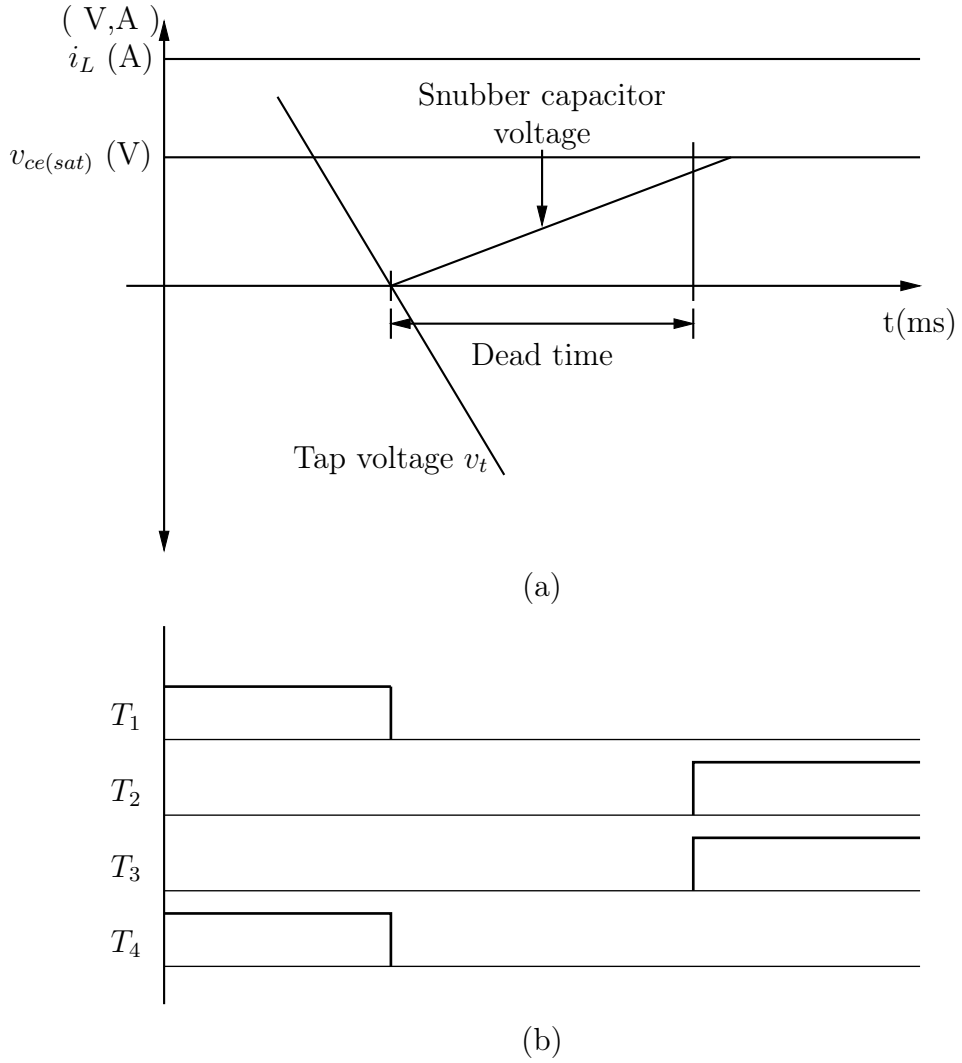

Figure 4.13: (a) Voltage and current waveform for the snubber capacitor; (b) IGBT gating signals.

an alternative current path, as discussed earlier. The capacitor voltage rises linearly, as the constant inductor current flows through the capacitor for the entire duration of the dead time. The main design principle is to limit the capacitor voltage to remain lower than the saturation voltage of IGBTs T_2 and T_3, when the IGBTs switch-on.

The worst case scenario accounts for the voltage, current and time duration during which the snubber capacitor will operate, and for the switching behaviour of the IGBTs. These three variables (voltage,current and time) are listed below, together with a description of how each value is determined for use in the design equation.

- Capacitor voltage: The maximum voltage that the capacitor may reach

during the conduction period, after the dead time has elapsed, must be limited for one specific reason. This maximum voltage must be lower than twice the saturation voltage $V_{ce_{(sat)}}$ of the IGBTs. If this condition is not met, IGBTs T_2 and T_3 will short-circuit the snubber capacitor when they turn-on. If the voltage over the capacitor is lower than twice the saturation voltage of the IGBTs, however, the IGBTs will limit the current flowing through the IGBTs due to the low collector-emitter voltage.

- Capacitor current: The capacitor must be designed for the worst case scenario during which the current it conducts will be the largest. The worst case is during the dead time period, after the zero crossing of the input voltage v_s with the largest possible phase between the input voltage and the inductor current.

- Time duration: The conduction period of the snubber capacitor in this situation is governed solely by the dead time. The time duration of the dead time determine the conduction period of the snubber capacitor.

- IGBT behavior: It is nearly impossible to determine the exact amount of current that will flow through the capacitor if the non-ideal switching behavior [13] of the IGBTs must be accounted for. It is thus assumed that the switching behavior of the IGBTs is ideal to the extend that they switch-off completely directly after the gating signal has been removed.

Calculating the capacitance of the snubber capacitor is accomplished by using (4.5.1) [14] while taking into account the considerations listed above as reference for setting the values of the equation.

$$C_s = \frac{idt}{dv} \tag{4.5.1}$$

4.6 Summary

This chapter derived all the equations that were required to design the various components of the IGBT-based tap changer and to calculate the relevant losses, and specifically the conduction and switching losses. A heat sink design was presented that determines the maximum switching frequency that can be achieved for a chosen heat sink and IGBTs. Lastly, the design equations for the filter components of the IGBT-based tap changer were derived, in addition to those dealing with the capacitance of the snubber capacitor.

Chapter 5

Design implementation

The main objective of this chapter is to implement the designs presented in Chapter 4 for a specific transformer and specific system ratings. These ratings determine the ratings of the IGBTs, thyristors, capacitors and inductors. The list presented below provides an overview of the chapter layout, briefly summarising each section.

- Implementing the IGBT-based tap changer onto an autotransformer: An autotransformer is able to provide an additional voltage source, as required by the IGBT-based tap changer. The connection of the IGBT-based tap changer to the autotransformer is discussed, as well as the connection of the IGBT-based tap changer to either a single-phase or a three-phase system.
- IGBT selection and performance analysis: This section presents a range of IGBTs that could be implemented into the IGBT-based tap changer. A specific IGBT is chosen and its performance in the IGBT-based tap changer is verified.
- Thyristor selection: The selection of the correct thyristors is discussed, together with the required parameters that influence the selection process.
- Filter component design: The design of the passive components used to perform the filtering in the IGBT-based tap changer is covered in this section.
- Snubber capacitor design: The correct capacitance for the snubber capacitor is calculated in this section.
- Efficiency calculations: The chapter concludes by calculating the efficiency of the IGBT-based tap changer.

5.1 Integrating the IGBT-based tap changer with an autotransformer

The autotransformer used to provide the series winding required by the IGBT-based tap changer is a Cooper Power VR-32 voltage regulator [3]. This single-phase mechanical tap changer, which makes use of an autotransformer to provide the taps for the tap changer. Table 5.1 summarises the ratings of the VR-32 voltage regulator.

Description	Value
Power	220 kVA
Load current	100 A_{RMS}
Voltage (line-to-line)	22 kV_{RMS}
Basic insulation level (BIL)	150 kV
Maximum series winding voltage	10 % of input

Table 5.1: Transformer ratings.

The main reason for using the Cooper Power VR-32 regulator is the autotransformer that is used inside it. By means of 8 tap positions, the tap changer inside the VR-32 regulator is able to regulate the output voltage. On the downside, though, the mechanical nature of the tap changer raises its maintenance costs. The IGBT-based tap changer designed in this report is conceived as an add-on replacement to the mechanical tap changer used inside the VR-32 voltage regulator.

The autotransformer, which provides the additional voltage tap inside the VR-32 voltage regulator, is rated at 220 kVA. Connecting the VR-32 voltage regulator to a load that must be regulated with a 10 % voltage regulation range results in an additional tap voltage of 2 200 V. Together with a maximum load current of 100 A, it results in the autotransformer being rated at 220 kVA. In other words, this VR-32 voltage regulator is capable of regulating a single-phase load of up to 2.2 MVA connected to a 22 kV system with 100 A load current. This shows that it requires an autotransformer rated at only 10 % of the load power to regulate the relevant load; these are significantly more economical as well as being smaller in size. Building the IGBT-based tap changer into a separate weatherproof container allows the container to be mounted directly onto the VR-32 voltage regulator. This allows the IGBT-based tap changer to be installed in the field without necessitating any serious modifications to the VR-32 voltage regulator. Connecting the IGBT-based tap changer between the VR-32 regulator and the load is the only modification that is required to make to the high voltage connections of the VR-32. The only other necessary connection involves the control signals sent from the controller

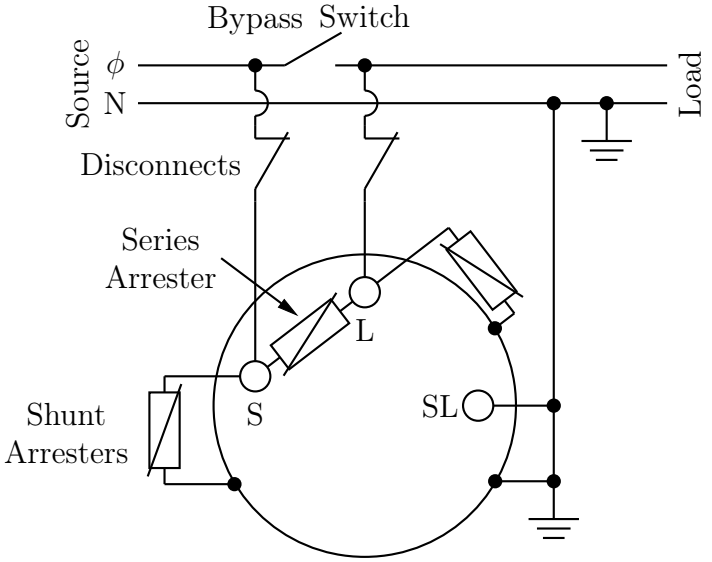

Figure 5.1: Connection diagram [3] for the Cooper Power VR-32 voltage regulator to a single-phase system.

of the IGBT-based tap changer to the controller of the VR-32 voltage regulator to operate the reversing switch of the tap changer.

Figure 5.1 shows how to connect the VR-32 voltage regulator to a single-phase source. The source connects in front of the bypass switch through a disconnect switch to the source (S) bushing of the voltage regulator. Connect-

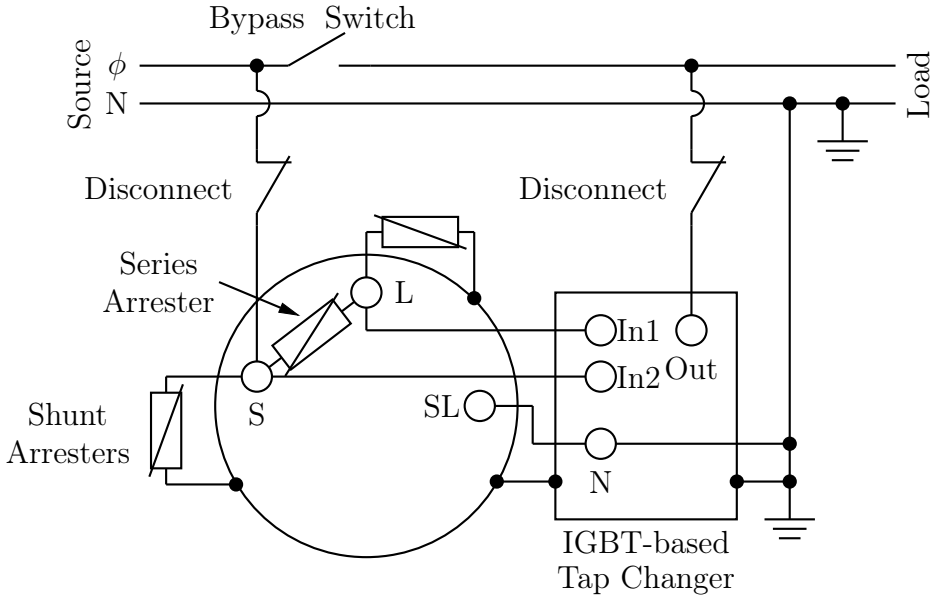

Figure 5.2: Connection diagram for the Cooper Power VR-32 voltage regulator connected to the IGBT-based tap changer for use in a single phase system.

ing the load (L) bushing to the load side of the bypass switch by means of a disconnect switch allows the VR-32 voltage regulator to regulate the load voltage while the source voltage varies. The SL bushing of the VR-32 voltage regulator connects to the neutral of the single-phase system. Making use of the bypass switch together with the two disconnect switches make it possible to do maintenance on the VR-32 voltage regulator without interrupting the power supply to the load for long durations of time.

As already stated, it is straightforward to connect the IGBT-based tap changer to the VR-32 voltage regulator. This is illustrated in Figure 5.2. Most of the original connections used for the VR-32 voltage regulator itself can be retained. Connecting the source (S) and load (L) bushings of the voltage regulator to the (In1) and (In2) bushings of the IGBT-based tap changer supplies the IGBT-based tap changer with the required input voltages. The neutral of the system connects to the (SL) bushing of the VR-32 voltage regulator and to the neutral bushing of the IGBT-based tap changer. Connecting the output (Out) bushing of the IGBT-based tap changer through the disconnect switch to the load allows the IGBT-based tap changer to supply power to the load. Bypassing the IGBT-based tap changer connected to the VR-32 voltage regulator can still be done by opening the disconnect switches and closing the

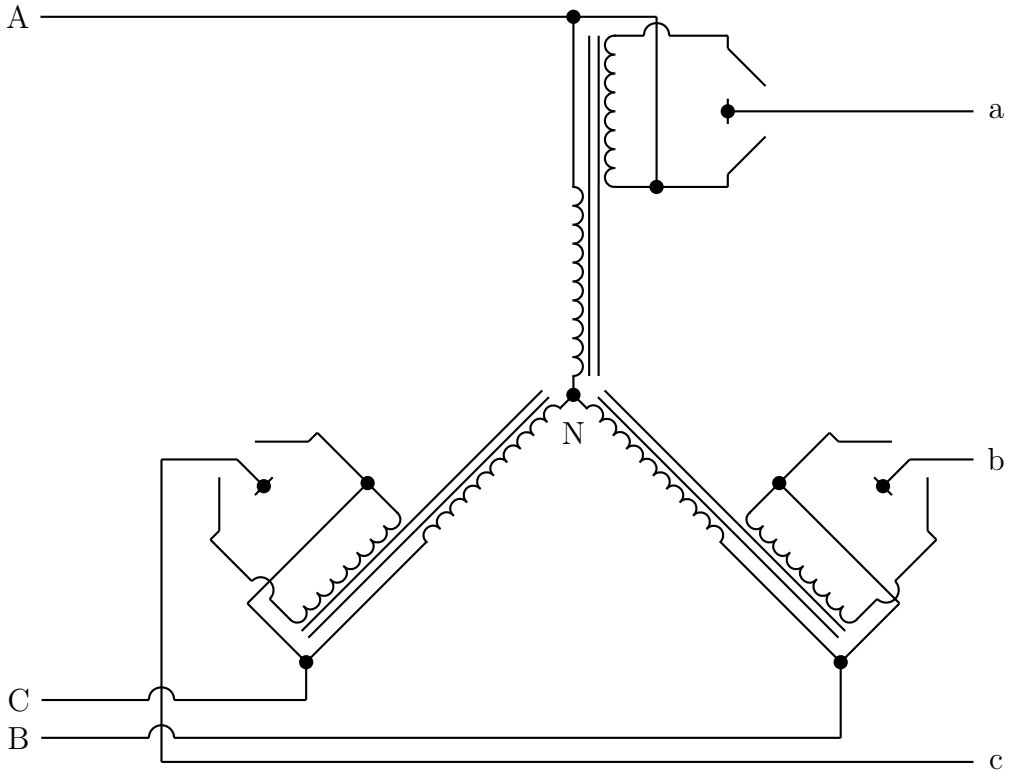

Figure 5.3: Implementation of three single-phase IGBT-based tap changers in a star configuration.

bypass switch.

The system for which the IGBT-based changer is designed is an 11 kV_{LL} rated system. Initially designed for a single-phase system, the design system voltage can be 6 351 V. But adding two further IGBT-based tap changers in a star configuration, as shown in Figure 5.3, allows the single-phase version to be implemented directly without needing to redesign the system. Communication between the different tap changers for each is additionally required for protection.

5.1.1 Series winding leakage inductance calculation

In order to design the compensator used in the feedback controller, the leakage inductance of the series winding of the autotransformer must be determined. Using the leakage inductance in the design of the compensator allows the compensator to compensate for it.

Determining the leakage inductance of the autotransformer requires the equivalent circuit model of the autotransformer to be modelled. The equivalent circuit model for a normal two-winding distribution transformer is shown in Figure 5.4.a [15].

R_{CL} refers to the iron losses in the core as a resistance and jX_m refers to the magnetizing reactance. R_1 and jX_1 provide the primary winding resistance and leakage reactance, whereas R_2 and jX_2 are the secondary winding resistance and reactance.

The difference between the connections of a two-winding transformer and an autotransformer lies in connecting the secondary winding to the primary winding. Connecting the bottom terminal of the secondary winding to the input terminal on the primary creates a boosting autotransformer (see Figure 5.4.(b))[15]. There as some disadvantages with this connection with regard to the two-winding transformer, with the most important one being the loss of the magnetic or galvanic isolation between the primary and the secondary windings. The advantage of connecting a two-winding transformer in this manner is that the transformer only transforms the power needed for the secondary winding (which is known as the series winding in an autotransformer). The lower amount of power that needs to be transformed effectively allows the autotransformer to be smaller and therefore less expensive to manufacture. These advantages and disadvantages of the autotransformer mean that it is ideal for use on transmission networks.

Determining the leakage inductance of the autotransformer is done in the same manner as is used for a two-winding distribution transformer with the open circuit and short circuit tests [16]. The same procedures are used to determine the parameters for the autotransformer but the circuit model in Figure 5.4.(b) is first redrawn into the equivalent circuit model (See Figure 5.5)[15] for a boosting autotransformer.

R_{CL} refers to the iron losses in the core as a resistance, whereas jX_m is the magnetizing reactance. E_s and E_c represent the voltages of the windings, with E_s the series winding voltage and E_c the common winding voltage. R_c and R_s are the winding resistance for the common and series winding respectively, while jX_c and jX_s are the winding leakage reactances for the common and series windings respectively.

Performing the open circuit test on the autotransformer with no load connected to the output, as shown in Figure 5.6 of the autotransformer, results in most of the current flowing through the shunt impedance that consists of R_{CL} and jX_m.

Applying the full rated voltage to the input terminal of the transformer while measuring the input current and active power provides sufficient information to determine R_{CL} and jX_m. If one assumes that very little or no current flows through the common winding with all the current measured going through R_{CL} and jX_m, then the calculations are simplified.

Using (5.1.1) allows the apparent power absorbed by the core to be deter-

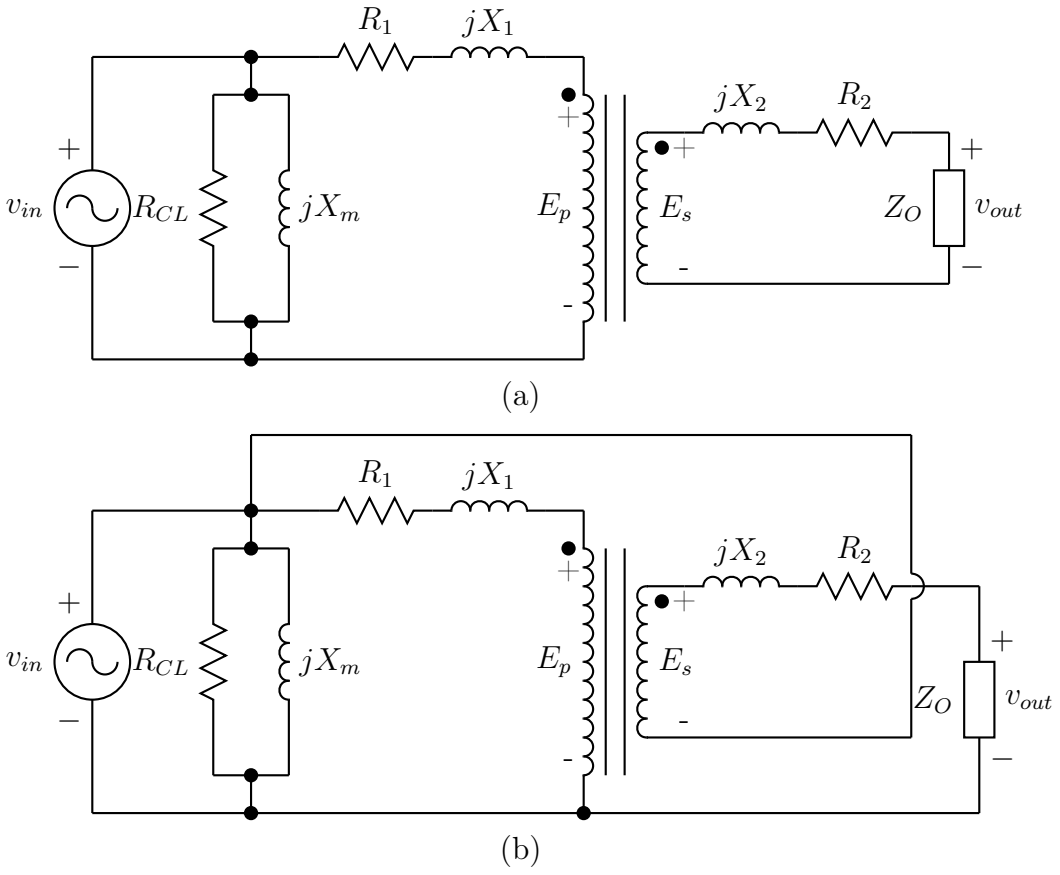

Figure 5.4: Circuit models for power transformers: (a) Two-winding distribution transformer; (b) Connection of a two-winding transformer to operate as a boosting autotransformer.

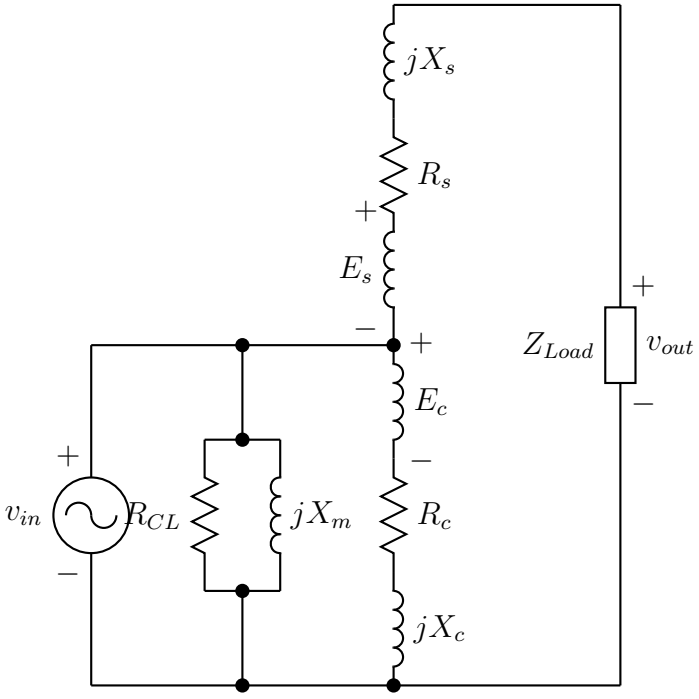

Figure 5.5: Equivalent circuit diagram for a boosting autotransformer.

mined.

$$S_m = V_o I_o \tag{5.1.1}$$

This allows the reactive power absorbed to be determined by means of (5.1.2):

$$Q_m = \sqrt{S_m^2 - P_o^2} \tag{5.1.2}$$

The active power is measured with a power meter and the reactive power is determined by means of (5.1.2). The iron losses in the core are calculated with (5.1.3) and the magnetizing reactance with (5.1.4).

$$R_m = \frac{V_o^2}{P_o} \tag{5.1.3}$$

$$X_m = \frac{V_o^2}{Q_m} \tag{5.1.4}$$

The short circuit test can be used to determine the parameters for the common and series windings. This test starts by connecting the input of the autotransformer to a variable voltage source with the source set to 0 V. Then the output of the series winding is connected through an ampere meter to the neutral, which results in short-circuiting the series winding of the autotransformer. Starting the test by increasing the input voltage from zero will

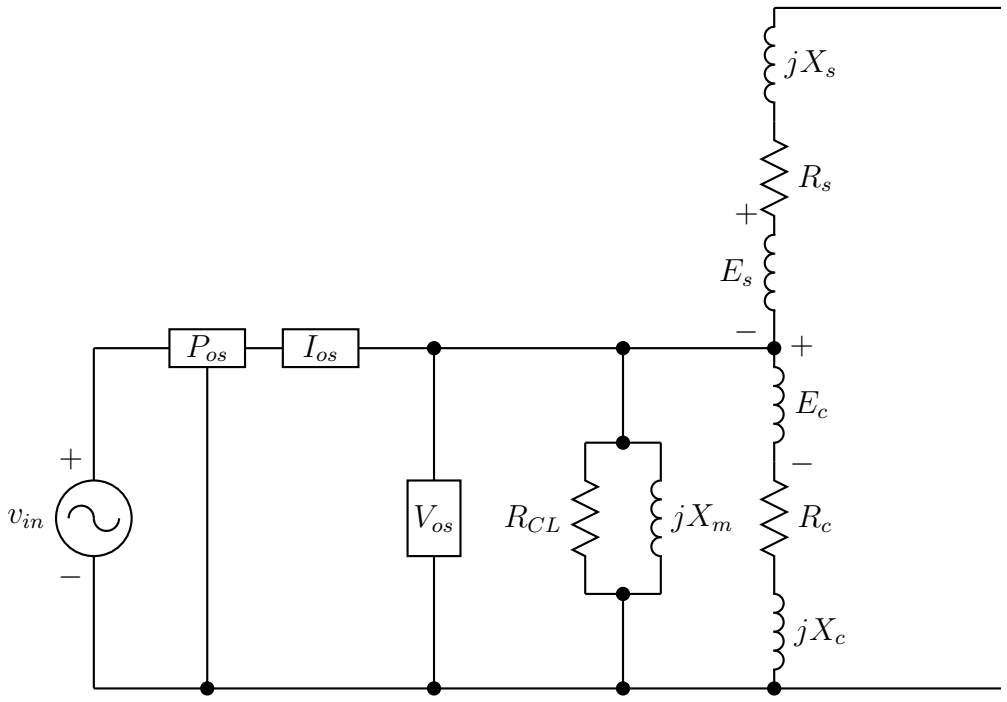

Figure 5.6: Circuit diagram showing the connections of the common winding and the series winding together with the voltage meter V_o, current meter I_o and active power meter P_o used for the open circuit test.

result in large amounts of current to flow through the series and common windings. Limiting the amount of current flowing through the series winding below the maximum rated current of the winding prevents the windings from being damaged.

Measuring the input voltage, current and active power as shown in Figure 5.7, as well as the short-circuit current, allows the winding parameters for the common and series windings to be determined.

Using the input voltage and current measurements V_{sc} and I_{sc} to calculate the apparent power with (5.1.5) delivers the reactive power into the autotransformer with (5.1.6).

$$S_{sc} = V_{sc} I_{sc} \tag{5.1.5}$$

$$Q_{sc} = \sqrt{S_{sc}^2 - P_{sc}^2} \tag{5.1.6}$$

Calculating the winding resistance and leakage reactance with (5.1.7) and (5.1.8) respectively delivers the winding resistance and leakage reactance for both the common and series winding added together.

$$R_{sc} = \frac{V_o^2}{P_{sc}} \tag{5.1.7}$$

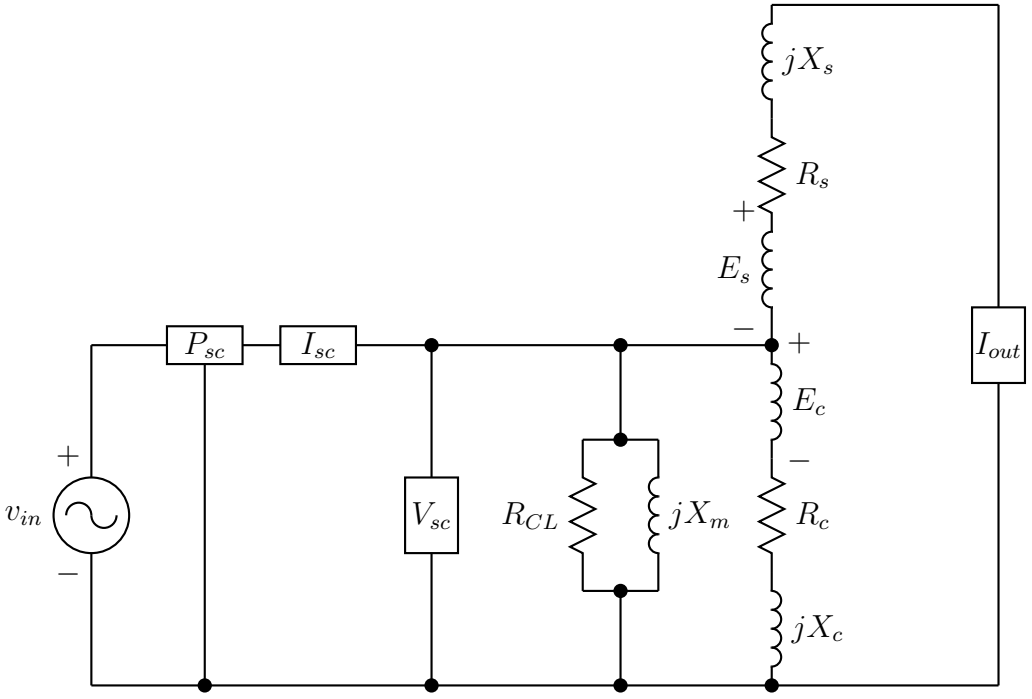

Figure 5.7: Circuit diagram of autotransformer for the short circuit test with P_{sc} the active power measurement input into the autotransformer, I_{sc} the current and V_{sc} the voltage measurements into the transformer, I_{out} the current measurement of the series winding current.

$$X_{sc} = \frac{V_o^2}{Q_{sc}} \tag{5.1.8}$$

However, using the difference between the series current measured with I_{out} and the input current provides a ratio that can be used to separate the series winding parameters from the common winding parameters with (5.1.9).

$$a_I = \frac{I_{out}}{I_{sc}} \tag{5.1.9}$$

The common and series winding resistances can be determined by means of (5.1.10) and (5.1.11), whereas (5.1.12) and (5.1.13) provide the common and series winding reactances.

$$R_c = R_{sc} a_I \tag{5.1.10}$$

$$R_s = R_{sc}(1 - a_I) \tag{5.1.11}$$

$$X_c = X_{sc} a_I \tag{5.1.12}$$

$$X_s = X_{sc}(1 - a_I) \tag{5.1.13}$$

With the series winding reactance now known, (5.1.14) [14] can be used to determine the leakage inductance of the series winding.

$$L_s = \frac{X_s}{2\pi f} \tag{5.1.14}$$

The value for the leakage inductance of the series winding calculated with (5.1.14) is not 100 % accurate because of various unknown factors, which may influence these measurements. This value is however sufficiently accurate to be used for the compensator design in Chapter 7.

Determining the leakage inductance for the Cooper power VR-32 voltage regulator through the method mentioned above is not currently possible because the autotransformer is not connected. The leakage inductance is thus calculated by using autotransformer rated values for 100% load. The average impedance for the Cooper power autotransformer is 2 % [17] for the specific rated load applied to the autotransformer, as calculated by means of (5.1.15).

$$\begin{aligned} Z_{average} &= 0.02\frac{V_{operate}}{I_{operate}} \\ &= 0.02\frac{6\ 351\ V}{100\ A} \\ &= 1.270\ \Omega \end{aligned} \tag{5.1.15}$$

Assuming [17] that the real part of the Z equals the imaginary part results in (5.1.16):

$$\begin{aligned} Z_{average} &= X + Xj \\ |Z_{average}| &= \sqrt{X^2 + X^2} \\ &= \sqrt{2}X \\ X &= \frac{Z_{average}}{\sqrt{2}} \\ &= 0.898\Omega \end{aligned} \tag{5.1.16}$$

With the total reactance of the autotransformer at 0.635 1 Ω, the transformation factor can be used to determine the series winding reactance from the total reactance. The transformation factor is the factor at which the voltage is transformed from the common winding to the series winding; it is calculated with (5.1.17) [15].

$$\begin{aligned} a_T &= \frac{v_{in}}{v_t} \\ &= \frac{6\ 351}{635.1} \\ &= 10 \end{aligned} \tag{5.1.17}$$

The series winding leakage reactance is thus calculated by dividing the total leakage reactance of the autotransformer by the transformation factor, which results in a leakage reactance of 0.089 8 Ω for the series winding. Using (5.1.14) delivers the series winding leakage inductance of 285.85 μH. This value is the final value that was used to design the compensator for this thesis but the value is only an estimated value and not an actual measured value and thus cannot be used for practical designs.

5.2 IGBT selection and performance analysis

Selecting the IGBTs to be used for the IGBT-based tap changer depends on two major factors. One is the required blocking voltage and the other is the amount of current to be conducted by the IGBTs.

With the series winding of the autotransformer providing the additional voltage source as required by the IGBT-based tap changer, the required blocking voltage of the IGBTs is lowered. A line-to-neutral input voltage v_{in} of 6 351 V_{RMS} together with a 10 % higher series winding voltage of 6 986.1 V_{RMS} results in a tap voltage v_t of 635.1 V_{RMS}. However, the required peak voltage that the IGBTs have to block is 899 V_{peak}. As a result, IGBTs with a voltage rating greater than 900 V had to be chosen.

The IGBT models with blocking voltages higher than the required 900 V are grouped in Table 5.2 below according to their respective blocking voltages. The list contains all the blocking voltages for the different IGBTs, as well as indicating the respective manufacturers. A few parameters are listed too, thus providing a brief overview into the capabilities of the available high power IGBTs.

IGBT	Manufacturer	Model number	Test voltage
6 500 V	INFINEON	FZ400R65KF2 [8]	3 600 V
4 500 V	MITSUBISHI	CM400HB-90H [18]	2 250 V
3 300 V	EUPEC	FZ400R33KL2C_B5 [19]	1 800 V
1 700 V	SEMIKRON	SKM600GA176D [20]	1 200 V

Table 5.2: High power IGBT models and manufacturers.

All the IGBTs listed above are packaged in a module together with an anti-parallel diode. The blocking voltage of each IGBT indicates only the maximum voltage that the IGBT can block without operating. This voltage rating is used primarily to categorize the IGBTs and not to provide any data that may be useful when choosing an IGBT. Each IGBT is tested to ascertain its performance characteristics, and these tests provide the data that is ultimately used to choose the suitable IGBTs.

The decision of which IGBT to use depends on the test voltage and current of each IGBT. Since the maximum tap voltage v_t that the IGBT must block is 899 V, any of the IGBTs may be suitable for use in the IGBT-based tap changer, but a safety margin must be allowed for. A suitable safety margin would allow some voltage ripple to be present over the IGBTs while switching caused by the filter capacitors conducting the inductor current. A specific value for the safety margin cannot be given, however, and the safety margin provided by the chosen IGBT must be verified ny means of testing and simulation. Implementing any of the IGBTs from the 3 300 V IGBT and higher will work, but is expensive. The 1 700 V IGBT provides a safety margin of 300 V or 33 % while being the least costly of all the IGBTs; as a result, the 1 700 V IGBT was the first choice for implementation.

Table 5.3 shows all the additional parameters of the IGBTs while Table 5.4 describes the symbols used.

Symbol	6 500 V	4 500 V	3 300 V	1 700 V
IGBT specifications				
I_c	400 A $T_C = 80°C$	400 A $T_C = 85°C$	400 A $T_C = 80°C$	470 A $T_C = 80°C$
$V_{ce(sat)}$	5.3 V $T_j = 125°C$	3.3 V $T_j = 125°C$	3.7 V $T_j = 125°C$	2.45 V $T_j = 125°C$
E_{on}	4 000 mJ $T_j = 125°C$	2 000 mJ $T_j = 125°C$	1 200 mJ $T_j = 125°C$	255 mJ $T_j = 125°C$
E_{off}	2 300 mJ $T_j = 125°C$	1 250 mJ $T_j = 125°C$	600 mJ $T_j = 125°C$	155 mJ $T_j = 125°C$
$R_{th_T(j-c)}$	0.017 K/W	0.021 K/W	0.0255 K/W	0.044 K/W
Diode specifications				
V_F	3.9 V $T_j = 125°C$	4.0 V $T_j = 125°C$	2.25 V $T_j = 125°C$	1.6 V $T_j = 125°C$
I_F	400 A $T_C = 80°C$	400 A $T_C = 85°C$	400 A $T_C = 80°C$	410 A $T_C = 80°C$
$R_{th_D(j-c)}$	0.032 K/W thermal resistance	0.042 K/W	0.051 K/W	0.09 K/W
Module specifications				
$R_{th_M(c-s)}$	0.0125 K/W	0.015 K/W	0.061 K/W	0.038 K/W

Table 5.3: List of all the additional parameters for each of the IGBTs

Symbol	Description
I_c	IGBT maximum on-state collector current
$V_{ce(sat)}$	Collector-emitter saturation voltage
E_{on}	Switch on energy
E_{off}	Switch off energy
$R_{th_T(j-c)}$	IGBT junction-to-case thermal resistance
V_F	Diode on-state forward voltage
I_F	Maximum diode forward current
$R_{th_D(j-c)}$	Diode junction-to-case thermal resistance
$R_{th_M(c-s)}$	Module case-to-sink thermal resistance

Table 5.4: Descriptions of the symbols used in Table 5.3.

It is clear from these parameters that the 1 700 V IGBT presents the best solution for use in the IGBT-based tap changer. The main factors contributing to this decision were the turn-on and turn-off energy losses, which are considerably lower for the 1 700 V IGBT than for the others. The switching losses generated by the IGBTs by these turn-on and turn-off energy losses result in heat, which has to be conducted away from the junction of the IGBT. In addition, it influences the switching frequency of the IGBT-based tap changer.

The only other factor that must be considered is the thermal resistance of the IGBTs. As the 1 700 V IGBT has a thermal resistance that is higher than those of the other IGBTs, it cannot conduct the same amount of heat away from the junction than the other IGBTs can, which results in a lower operating junction temperature. But the low switching losses generated by the 1 700 V IGBT, mean that this IGBT is nonetheless superior to the other IGBTs, even though its thermal resistance is the highest.

Tests to confirm the performance of the IGBT-based tap changer while operating with the selected 1 700 V IGBT have verified that this IGBT is adequate for the design. Using the equations derived in Chapter 4 to calculate the switching and conduction losses, makes it possible to determine the theoretical amount of heat generated by the IGBT, which influences the maximum switching frequency. The performance analysis conducted in the next section looks at more specifically at the switching and conduction losses for the specified parameters.

5.2.1 1 700 V IGBT performance

The operating parameters of the IGBT-based tap changer are listed in Table 5.5 below. These values are used by the design equations to determine the switching and conduction losses generated by the IGBTs.

Description	Symbol	Value
Peak tap voltage	V_t	899 V
Peak collector current	I_O	141 A
Phase shift	ϕ	$\pm$1.047 rad/s ($\pm$60°)
Normalized switching energy	E	854.167 nJ
Switching frequency	f_s	10 kHz

Table 5.5: IGBT operation ratings.

The normalized switching energy for the 1 700 V IGBT is calculated by means of (4.2.2)[1] in Chapter 4.

The maximum peak voltage that the IGBTs are required to switch is 899 V, together with a maximum required peak current of 141 A. The maximum

[1]See page 42

switching losses generated in IGBTs T_1 and T_2 only occur with a zero phase shift between the peak collector current and the peak tap voltage. Changing the phase shift away from zero results in the switching losses decreasing in T_1 and T_2, while increasing in T_3 and T_4. This can be seen in Figure 5.8, which is based on (4.2.10) to (4.2.13)[2] in Chapter 4.

The top graph shows the switching losses generated by IGBTs T_1 and T_2 individually, while the bottom graph shows the switching losses for T_3 and T_4 individually. IGBTs T_1 and T_2 never generate switching losses at the same time due to the switching scheme; the same holds true for T_3 and T_4.

However, the IGBT generating the switching losses is also generating conduction losses while it is conducting the inductor current i_L together with another IGBT or diode. The conduction losses generated in any component are affected by the duty cycle of the PWM; in other word, in the conduction losses are effectively controlled by the duty cycle. Figure 5.9 shows the conduction losses generated in all the IGBTs and diodes as the duty cycle sweeps from 0% to 100%.

Figure 5.9 was drawn by using (4.1.3) to (4.1.6)[3] in Chapter 4.

[2]See page 43
[3]See page 38

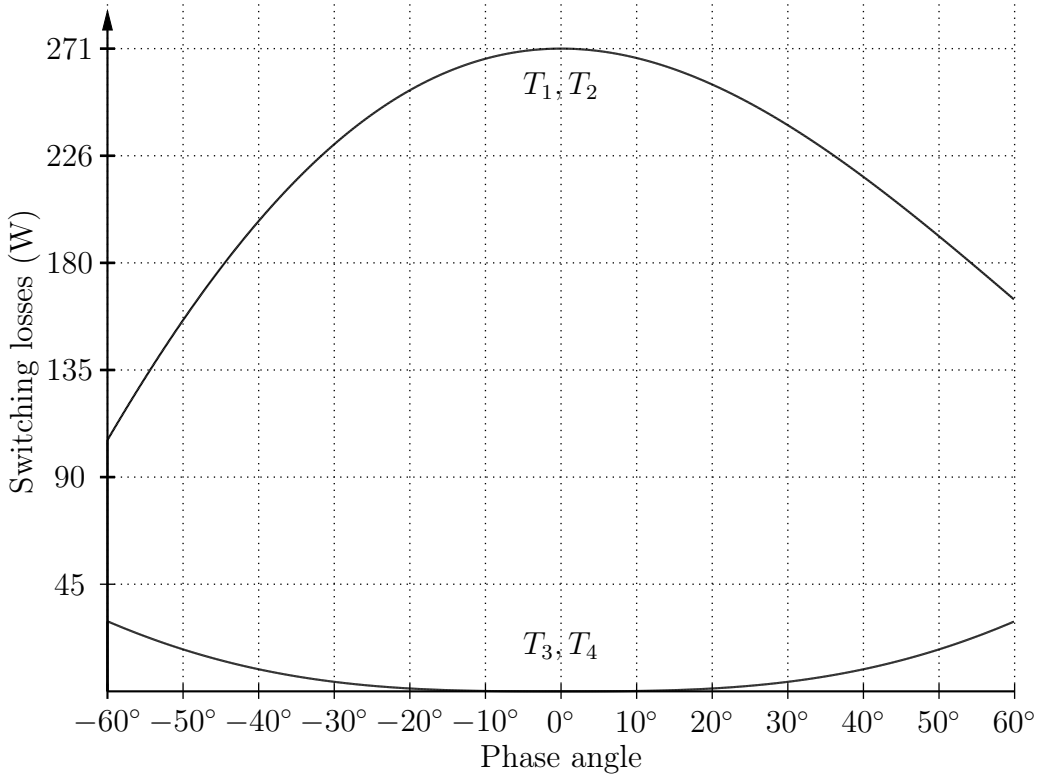

Figure 5.8: Switching losses generated by T_1,T_2,T_3 and T_4 as the phase shift changes from $-60°$ to $60°$.

The only other factor that influences the amount of losses generated (except for the load current) is the switching frequency. In other words, changing the switching frequency changes the amount of switching losses generated by the IGBTs. Higher switching frequencies generate more losses, as indicated in Figure 5.10.

The maximum amount of losses generated at any moment must be calculated by taking into account the switching scheme and the operating parameters of the IGBT-based tap changer. In a worst case scenario, the IGBT-based tap changer operates at rated capacity of 100 A_{RMS} with the duty cycle set at 100% and the switching frequency at 10 kHz. Adding the switching losses and conduction losses for IGBT T_2 as well as the conduction losses of D_1 determines the maximum amount of losses to be 452.45 W.

Using a Semikron PX16 [21] heat sink with a thermal resistance of $R_{th_{sink}(s-a)}$ = 0.025 K/W results in a maximum switching frequency of 14 300 Hz from (4.3.8)[4]. This results from a maximum sink temperature of $T_s = 64°C$ and an ambient temperature $T_a = 50°$C. With the maximum switching frequency being 4 300 Hz higher than the chosen switching frequency of 10 kHz, it creates a large safety margin, thus allowing the IGBT-based tap changer either to conduct more current or to operate at higher ambient temperatures. This

[4]See page 51

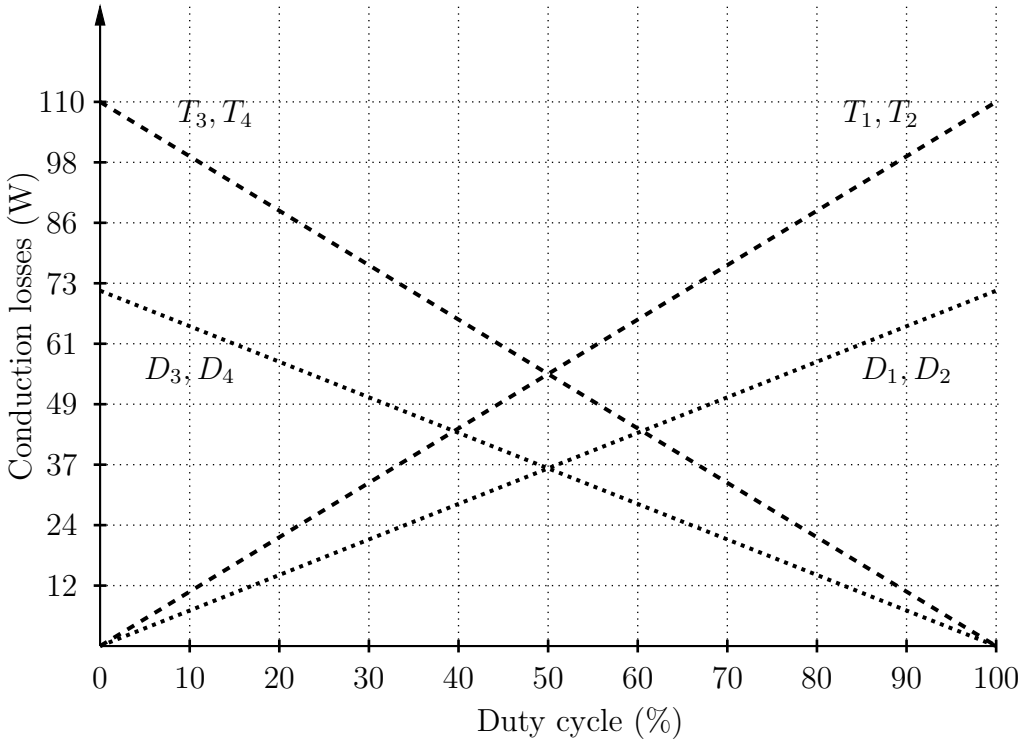

Figure 5.9: Conduction losses generated by IGBTs T_1,T_2,T_3 and T_4 and diodes D_1,D_2,D_3 and D_4 as the duty cycle changes from 0 % to 100 %.

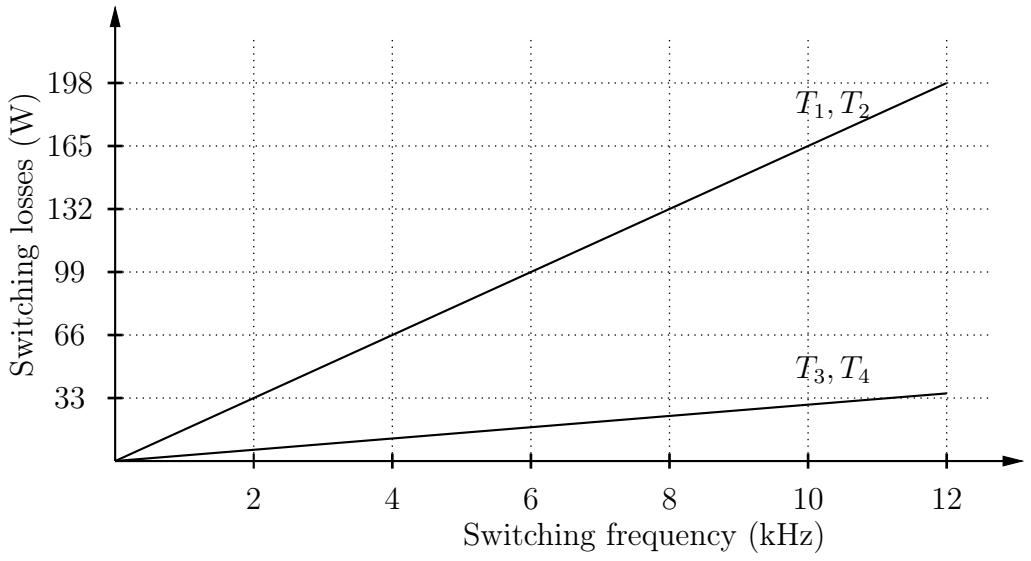

Figure 5.10: Switching losses generated by IGBTs T_1 and T_2 individually together with T_3 and T_4 individually, with the switching frequency rising from 0 Hz to 12 kHz with a phase shift of 60°.

can only be accomplished because of the lower switching losses generated by the IGBTs with the lower switching frequency.

As it is possible to operate the IGBT-based tap changer with a switching frequency below the maximum switching frequency by using the 1 700 V IGBTs, it confirms that this particular IGBT is the ideal choice for the design presented herein.

5.3 Thyristor selection

The selection of the thyristors used for the bypass switch is based on the amount of the current to be conducted by the thyristors. Normal current conduction scenarios include the conduction of the load current during periods when the load current exceeds the set current limit of the IGBT-based tap changer. The bypass switch also activates in another scenario, namely when the voltage over the bypass switch reaches dangerously high levels, thus forcing the break-over diodes to turn on the thyristors. However, it is not ideal to select a thyristor according to these conditions, since it does not make provision for extremely rare scenarios.

One such scenario may occur when the phase wire happens to touch the neutral wire due to some sort of obstruction at the load side of the IGBT-based tap changer. For instance, a broken tree branch that has fallen onto an overhead line, which connects the IGBT-based tap changer to the load, will short out the phase wire and the neutral, thus resulting in a phase-to-neutral fault. This fault generates a large fault current, which - if it is not rerouted away from the IGBTs - can damage these. Rerouting the fault current away from the IGBT occurs by means of thyristors S_1 and S_2, in the bypass switch(see Figure 2.3). The thyristors used in the bypass switch must also be able to conduct the large fault current for the entire duration of the fault . The fault current only stops flowing after the protection relays at the supply end of the power line have shut down the power line.

When the fault occurs, the fault current flowing through the IGBT-based tap changer changes the output current waveform to an unknown waveform. Because of this change, the selection of the thyristor cannot be based on using normal average current and voltage ratings. Instead, selection of an appropriate thyristor must be based on different parameters. Using the Joule integral [22] or i^2t rating specifies the amount of energy that can be conducted by the thyristor without it being damaged. The i^2t rating refers to the amount of energy dissipated in the thyristor in the form of heat for the entire conduction period. Selecting a thyristor with an i^2t rating that is higher than the required rating prevents the thyristor from possible damage that may occur due to fault currents.

It is specified [4] that the maximum fault current of 2 000 A must be conducted by the thyristor for a maximum time period of 0.8 seconds. Theoretically, the required i^2t value of the thyristor must therefore be 3 200 000 A^2s, or higher, which is a fairly high rating for any thyristor. The thyristor chosen for this project has a i^2t rating that is higher than the required rating: it is a SKET 740/22G 4H thyristor manufactured by Semikron (see ratings summarised in Table 5.6[23] below).

Two more elements have to be taken into consideration when using thyristors in the bypass. The critical rate of rise of the off-state or $\frac{dv}{dt}$ voltage determines the maximum rate at which the voltage over the thyristor may

Description	Symbol	Value
Maximum repetitive blocking voltage	V_{DRM}	2 200 V
Maximum continuous current	I_{TAV}	700 A
Surge Forward current	I_{TSM}	31 000 A
Maximum let-through energy	i^2t	6 480 000 A^2s (T_j=25°C)
Critical rise rate of off-state voltage	$(\frac{dv}{dt})_{cr}$	2 000 V/μs

Table 5.6: SKET 740/22G H4 thyristor operating ratings.

rise. If the voltage over the thyristor rises faster than the specified rate, it may result in the thyristor switching on without applying a gate signal. The rate at which the voltage rises over the thyristor will never reach the 2 000 V/μs rate under normal operating condition, due to the maximum tap voltage of 900 V peak. During fault situations between the load and the IGBT-based tap changer, however, provision must be made for the high voltage present over the thyristor due to the low load voltage. Using a MOV or a surge suppressor in parallel may provide enough protection but connecting more than one thyristor in series may also be a viable solution.

Another element that must be considered is the reverse recovery time of the thyristor. The reverse recovery time states the time it takes for remaining charge in the thyristor to dissipate, the thyristor only turns off completely after this occured. This value is not given in Table 5.6 because it was not reflected on the supplied data sheet. Switching on the IGBTs before the recovery time has passed for the thyristor may short the input voltage to the tap, causing dangerous currents to flow, which may damage the IGBTs. In order to prevent this from happing, a delay must be implemented to allow the reverse recovery time of the thyristor to pass, before the IGBTs are switched on again.

5.4 Filter component design

In this section, the required capacitance and inductance of the three components C_1, C_2 and L_O, which perform the filtering inside the IGBT-based tap changer, are calculated. Given the switching frequency, which has been verified at 10 kHz, it is possible to determine the inductance of the output filter inductor L_O. Using (4.4.4)[5] in Chapter 4 determines the inductance for inductor L_O.

In order to calculate the inductance of the inductor the worst case scenario under which the inductor operates must be defined. The maximum voltage difference over the inductor reaches V_T = 899 V, which is the peak value of tap voltage v_t.

[5]See page 55

The ripple component of the inductor current is determined by the inductance of the inductor. Low inductance values allow the ripple component to become large, whereas high inductance values make the ripple component smaller. Higher inductance values, however, influence the physical size of the inductor. An even middle ground must be reached between the magnitude of the ripple component Δ_{i_L} of the inductor current and the inductance of the inductor.

The ripple component flows through the IGBTs as the switching continues, thus requiring the IGBTs to switch currents higher than the peak value of the load current i_O. But the select 1 700 V IGBTs have a maximum current conduction value of 400 A, which offers a large margin for the ripple component. Choosing the magnitude of the ripple component of the inductor to be no larger than 30% of the peak value of the load current i_O results in a maximum inductor current of 183.3 A. In this case, the current is over 200 A smaller than the maximum current of the IGBTs, proving that a 30 % ripple component is sufficient and that it makes the inductance of the inductor smaller. The complete magnitude of the ripple component Δ_{i_L} of the inductor current results in 84.6 A.

Adjusting the duty cycle also adjusts the magnitude of the ripple component, with a duty cycle of 50% delivering the largest ripple current. Using all the variables required for (4.4.4), as summarised below in Table 5.7, the inductance of the output inductor L_O will be 265.66 μH.

Description	**Symbol**	**Value**
Inductor voltage	V_T	899 V
Ripple component	Δ_{i_L}	84.6 A
Duty cycle	D	50 %
Switching frequency	f_s	10 kHz

Table 5.7: Inductor design variables.

Calculating the capacitance of capacitors C_1 and C_2 makes use of (4.4.2)[6] in Chapter 4.

$$C_1 = C_2 = \frac{18}{\omega^2 L_1} \tag{5.4.1}$$

Only two variables are required to solve (5.4.1), namely, the leakage inductance $L_1 = 202.159\mu$H for the series winding of the autotransformer, and the required cut-off frequency ω of the combined filter. Selecting the cut-off frequency at 5 000 Hz or 31 416 rad/s allows the fundamental frequency to pass through the filter while the harmonics are filtered out. The resulting capacitance is 90.2 μF, which cannot be realised using only one single capacitor.

[6]See page 55

However, connecting four EPCOS B25832-C6226-K9 [24] capacitors rated at 22 μF and 960 V_{RMS} in parallel for C_1 and C_2 individually, is able to meet these requirements.

5.5 Snubber capacitor design

The snubber capacitor is designed by means of (4.5.1)[7] in Chapter 4. Using the design guidelines as provided for the capacitor design as stipulated Chapter 4, the following values are used for the different variables listed in Table 5.8.

Description	Symbol	Value
Inductor current	i_{L_O}	92 A
Dead time	dt	5.05 μs
IGBT saturation voltage	$V_{ce(sat)}$	2.45 V

Table 5.8: Inductor design variables.

As a worst case scenario, a 30° phase shift is applied between the tap voltage and the inductor current while the load current is at its rated value. This results in a capacitor current of 70.71 A, but provision must be made for the ripple component of the inductor current, which is set at 30 % resulting in a maximum worst case capacitor current of 92 A.

The dead time is calculated by taking into account the switch-off delay time of the IGBTs, which is the time it takes for the IGBT to respond to the change in state of the gating signal. The dead time also takes into account the actual current fall time of the IGBT, while the final value that is taken into account is a safety margin. The values for these are listed in Table 5.9 below.

Description	Symbol	Value
IGBT switch-off delay time	$t_{d(off)}$	890 ns
IGBT current fall time	t_f	160 ns
Safety margin	SM	4 μs

Table 5.9: Dead time calculation values.

A 4 μs safety margin provides 4 times the time required for the IGBT to switch off, according to the values provided in the data sheet. The final dead time is thus calculated as 5.05 μs.

The saturation voltage of the IGBTs is 2.45 V and it is necessary for the maximum voltage that the capacitor may reach after the dead time period

[7] See page 58

has elapsed, to be lower than twice this voltage. This results in the final capacitor voltage to be chosen as 4 V, which is 0.9 V lower than twice the saturation voltage of the IGBTs, thereby providing a large safety margin. The safety margin can be verified by looking at the amount of current that can be conducted by the IGBT for a specific collector-emitter voltage in the data sheet. A collector-emitter voltage of 2 V per IGBT allows only 225 A of current to flow through the IGBT, which is more than half of the maximum current of the IGBT at 470 A.

Using (4.5.1) together with the design values discussed above results in a capacitance of 116.15 μF. This value is too large to be realized by means of a single capacitor, especially at the full 900 V tap voltage, at which the capacitor must operate. Consequently, it will require many capacitors to be connected in parallel to make up the required capacitance.

5.6 Efficiency calculations

The efficiency of the IGBT-based tap changer shows the amount of energy that is dissipated by the components used inside the IGBT-based tap changer. Higher efficiency ratings can only be accomplished by allowing less energy to dissipate inside the system.

In order to calculate the efficiency, all the losses generated in all the components inside the IGBT-based tap changer must be added together. But it is very difficult to accurately calculate the energy dissipated by the capacitors, the inductors, the autotransformer and the wiring. As a result, the efficiency was calculated only with regard to the losses generated by the IGBTs.

Calculating the losses of the autotransformer by means of (5.6.1) shows that the expected efficiency, of more than 99%, in respect of a modern distribution transformer, is indeed met.

$$\begin{aligned} \eta &= 100\ \% \frac{Load\ Power}{IGBT\ losses\ +\ Load\ Power} \\ \eta &= 100\ \% \frac{635.1\ kVA}{452.45\ W + 635.1\ kVA} \\ \eta &= 99.9288\ \% \end{aligned} \tag{5.6.1}$$

The maximum power, which can be delivered to a single-phase load by the system is 635.1 KVA because of the 6 351 V output voltage with a maximum current of 100 A. The IGBT losses have been calculated in Section 5.2.1[8].

The efficiency of the AC-chopper used inside the IGBT-based tap changer is shown below in (5.6.2).

[8]See page 71

$$\begin{aligned}
\eta &= 100\ \% \frac{Power\ converted}{IGBT\ losses\ +\ Power\ converted} \\
\eta &= 100\ \% \frac{v_t i_O}{IGBT\ losses + v_t i_O} \\
\eta &= 100\ \% \frac{635.1x100}{452.45\ W + 635.1x100} \\
\eta &= 99.29\ \% \qquad (5.6.2)
\end{aligned}$$

The efficiency of the IGBT-based tap changer connected to a single-phase 11 kV system is 99.9288%, while it is regulating a load of 635.1 kVA. This high percentage of efficiency can be attributed to the low losses generated by the IGBTs. The converted efficiency of 99.29% shows the efficiency of the AC-chopper that has been implemented to form the IGBT-based tap changer, which converts only 63.51 kVA of the power provided by the autotransformer. The converted efficiency is so small because of the 10 % tap voltage from the 6 351 V line-to-neutral voltage, which has resulted in a 635.1 V voltage rise together with 100 A of current flowing through the series winding of the transformer. This delivers a converted power of only 63.51 kVA, which is exactly 10 % of the load power.

5.7 Summary

This chapter has looked at the calculations that were used to determine the values of the different components implemented in the IGBT-based tap changer. The layout of the entire system was explored, especially with regard to the converter and the autotransformer, and it was examined how these would be implemented in a 3-phase system. The most appropriate IGBTs in the circumstances were selected and the losses were calculated, together with the maximum switching frequency that could be attained by the IGBTs for the chosen heat sink. The selection of the thyristors used in the bypass switched was covered. The values for the passive components, which include the filter components and the snubber capacitor, were calculated. The chapter finished by presenting the efficiency calculations for the entire system.

Chapter 6

Detailed hardware design

The main components covered in Chapter 2 are required by the IGBT-based tap changer to function. These high voltage and high current components in turn require additional circuit boards to function. The circuit boards discussed in this chapter connect all the small signal and low current signals between the high voltage components and the main controller board. Most of the signals connected between the controller board and the rest of the circuit boards do so through optical fibre cables, which provide isolation between the controller board and the other circuit boards. Figure 6.1 shows all the additional circuit boards connected to the high voltage components and the main controller board.

The list below gives a brief description of each of the additional circuit boards required for the correct operation of the IGBT-based tap changer.

- Controller board: The controller features many components, all of which are controlled by a single field-programmable gate array (FPGA). The FPGA generates all the control signals and receives all the measuring and detection signals.
- Sign detector board: The sign detector connects over all four of the IGBTs and detects the polarity of the tap voltage v_t. The sign detector acts as a hardware based solution that provides an accurate and vital signal required by the controller.
- IGBT driver boards: The gate drivers provide the required voltage and current for the IGBT to operate.
- Bypass switch driver board: The driver board used to operate the thyristors in the bypass switch supplies0 the required passive components to perform the over-voltage protection. The bypass switch driver also features the active components needed by the controller to operate the thyristors during over-current situations.

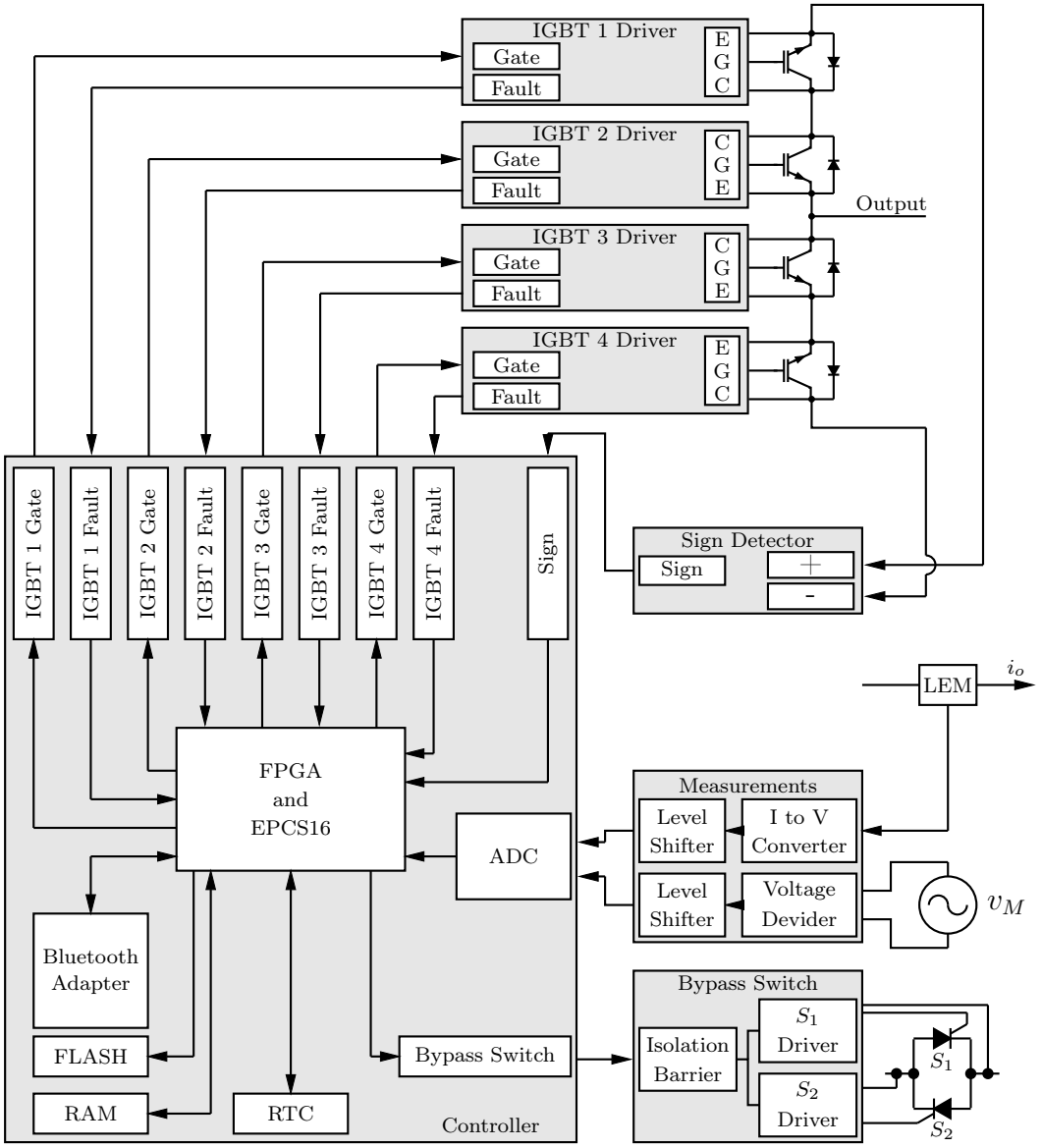

Figure 6.1: Layout of all the hardware used to control the key components in the tap changer.

- Measurement board: The measurement board features all the resistors and op-amps to deliver level shifted voltage and current measurements.

The PC boards discussed in this chapter was already designed prior to the start of this thesis for the scale-model IGBT-based tap changer used for the practical measurements in Chapter 9. Parts of this design were altered for use in the IGBT-based tap changer, however to make provision for the higher voltages and to improve performance.

6.1 Controller board

The controller board features a wide variety of components used to communicate with other circuit boards in the tap changer and with the outside world. Figure 6.2 [4] illustrates the layout of the controller board.

The list below contains a brief description of each of the components used on the controller board.

- FPGA: The FPGA forms the main component on the controller board. All the signals received by the controller board go directly to the FPGA. This uses these measurement, fault and sign signals to generate the PWM for the IGBTs.
- EPCS16: The EPCS16 stores the program code used by the FPGA when the controller board is powered down. The FPGA loads the program code directly from the EPCS16 after the controller board has powered up.
- FLASH: The Flash memory device serves as a non-volatile storage platform used to for logging purposes.

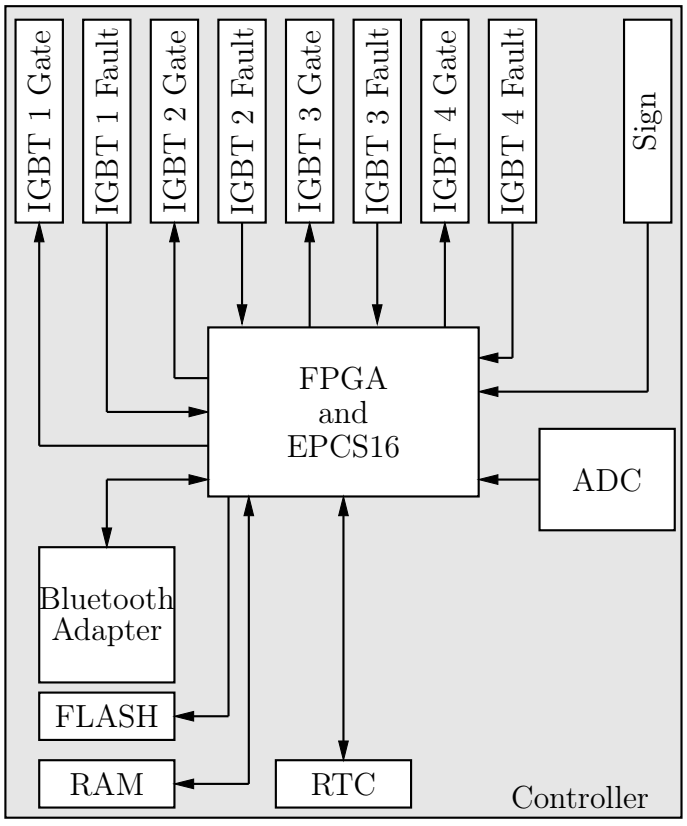

Figure 6.2: Component layout for the controller board.

- RAM: Random access memory (RAM) provides a fast access storage platform used by the FPGA to store data while operating.
- RTC: The real-time clock (RTC) provides accurate time and calendar dates to the FPGA. The FPGA makes use of the time and dates provided by the RTC for data logging.
- ADC: The analogue-to-digital converter (ADC) converts the analogue measurement signals into digital values, which the FPGA utilizes for calculations.
- Bluetooth adapter : The Bluetooth adapter allows the FPGA to communicate with the outside world through a wireless connection. Connecting with a computer gives the operator access to logged information and the operating parameters of the tap changer.
- Fibre optic transmitters: The fibre optic transmitters transmit control signals generated by the FPGA over optical fibre cables, this is accomplished by generating the signals for the optical fibres from the electrical signals sent by FPGA.
- Fibre optic receivers: The fibre optic receivers receive the fault signals from the IGBT driver boards as well as the sign signal from the sign detector via the optical fibres. The fibre optic receivers convert the signal sent over the fibre optics into electrical signals, which can be used by the FPGA.

The short summaries above only describe the purpose of each component on the controller board. The list below in Table 6.1 provides the name of the manufacturers plus the model number for the specific component used.

Component	**Manufacturer**	**Part number**
FPGA	Altera	EP3C25Q240
EPCS16	Altera	EPCS16N
FLASH	Advanced Micro Devices	A29L160D
RAM	Cypress Semiconducter	CY62157EV30LL-45ZSXI
RTC	Dallas Maxim	DS1302
ADC	Analog Devices	AD7924
Bluetooth	KC Wirefree	KC 11
Fibre optic TX	Avago Technologies	T-1521
Fibre optic RX	Avago Technologies	R-2521

Table 6.1: Controller board components.

6.2 Sign detector board

The sign detector [4] is one the most important components used in the IGBT-based tap changer. It send a signal to the controller board, informing it of the polarity of the tap voltage v_t over the IGBTs. The controller depends heavily on the signal received from the sign detector. The switching scheme depends on the signal received from the sign detector to such an extent that the IGBTs can be destroyed, if the signal from the sign detector fails or becomes inaccurate.

Figure 6.3 shows the basic component layout for the sign detector.

The list below briefly describes each of the components used to construct the sign detector, as shown in Figure 6.3.

- IC_1: The voltage comparator checks only if the voltage at the positive input terminal is larger or smaller than the voltage at the negative input terminal.
- Optical transmitter: The transmitter transmits the electrical signals applied to its terminals through the optical fibre cable to the controller board.
- Resistors R_4 and R_5: Both of these resistors consist out of 10 resistors connected in series. Conecting 10 resistors in series lowers the voltage over each resistor, allowing the use of standard sized resistors and not expensive high voltage resistors. The value of each individual series connection is calculated to limit the current that flows from the positive terminal of the tap voltage v_t to the negative terminal.

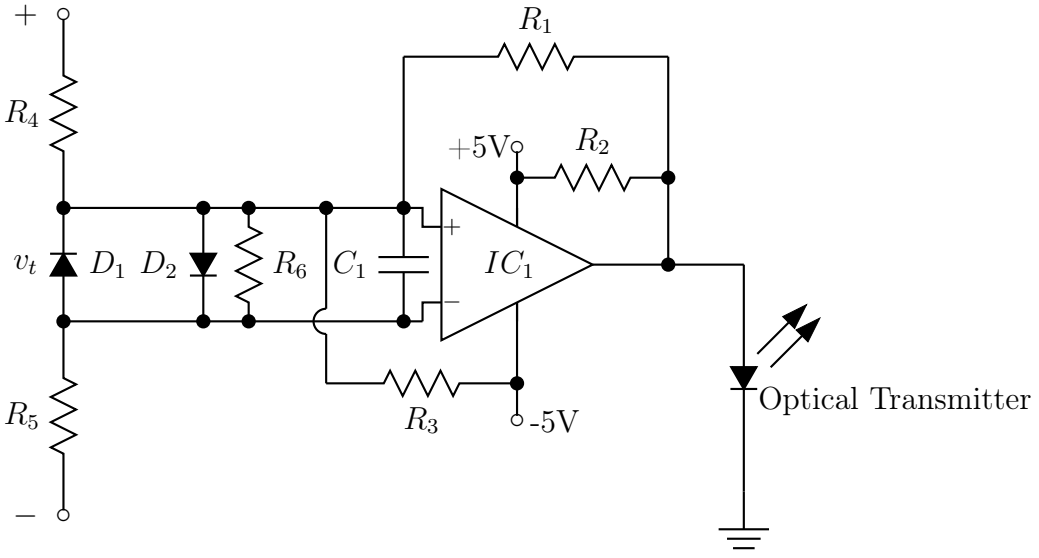

Figure 6.3: Component layout for the sign detector circuit [4].

- Diodes D_1 and D_2: These diodes limit the voltage applied to the terminals of the voltage comparator. The diodes start conducting the current flowing through resistors R_4 and R_5 as soon as the voltage over resistor R_6 reaches the forward voltage of the diodes.

- Resistor R_6: This resistor provides an alternative path for the current flowing through resistors R_4 and R_5. Resistor R_6 only conducts the current after diode D_1 or D_2 have switched off due to very low tap voltages.

- Resistor R_2: Resistor R_2 limits the current flowing through the optical transmitter or the voltage comparator while either conducts current.

- Resistors R_1 and R_3 with Capacitor C_1: These components dampen the oscillations in the voltage comparator [25] during the zero crossing of the tap voltage v_t using hysteresis.

The sign detector operates the optical fibre transmitter through the transistor inside the voltage comparator. The output of the voltage comparator activates during the period when the positive input terminal voltage exceeds the voltage at the negative input terminal. The positive terminal voltage exceeds the negative terminal voltage only during the positive half-cycle of the tap voltage.

The voltage comparator connects the output terminal to ground during the positive cycle of the tap voltage. The grounded output terminal of the comparator connects resistor R_2 as well as the optical transmitter to ground. The optical transmitter stops conducting current because both of the transmitter terminals connected to ground are forcing the transmitter to switch off. The switched off optical transmitter allows the current flowing through resistor R_2 to flow through the voltage comparator.

Figure 6.4.(a) shows the tap voltage while Figure 6.4.(b) shows the output of the sign detector.

The design of the passive components used in the sign detector is described in the following sections.

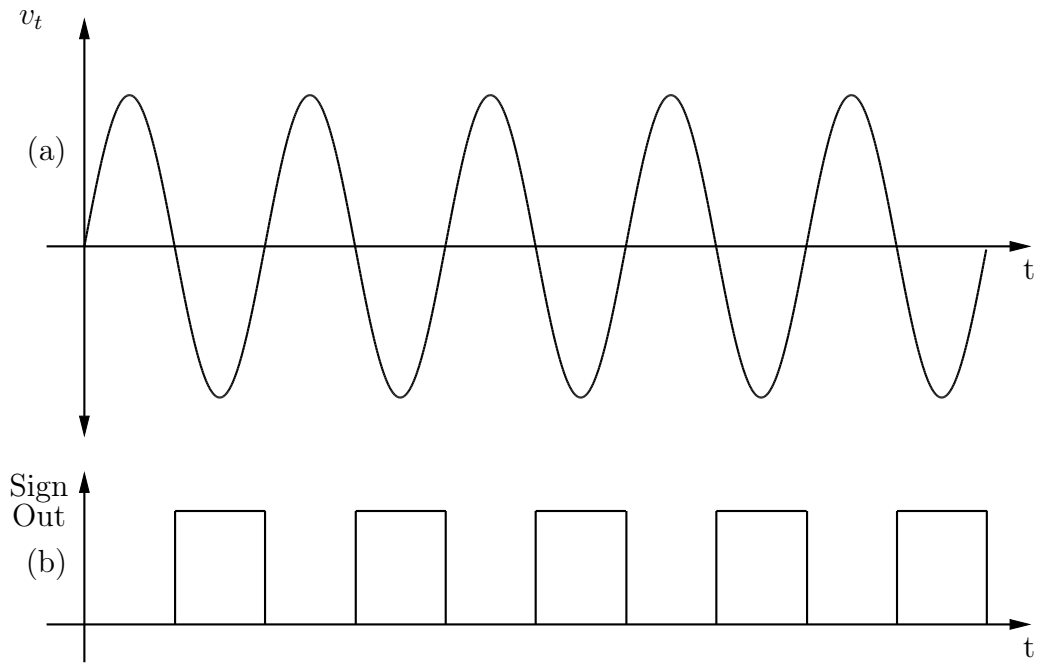

Figure 6.4: Output of sign detector; (a) Input voltage into sign detector measured at v_t; (b) Output provided to the controller by the sign detector.

6.2.1 Design of resistors R_4 and R_5

Resistors R_4 and R_5 consist of 10 resistors each, with all 10 connected in series. This series connection divides the tap voltage over all the resistors, thus reducing the voltage drop over each individual resistor. The power dissipation for each resistor remains small because of the small voltage drop over each resistor and the small current flowing.

The first step of the design was to calculate the voltage drop over each resistor. The 20 resistors connected between the terminals of the tap voltage v_t result in a voltage drop of:

$$v_R = \frac{\sqrt{2}v_{t_{RMS}} - v_{F_{D_1}}}{20} \tag{6.2.1}$$

With $v_t = 635.1\ V_{RMS}$ and $v_{F_{D_1}} = 0.95$ V the forward voltage of a ES1D diode used for D_1 delivers a voltage drop of 44.86 V over each individual resistor. Each individual resistor is capable of handling voltages over 100 V over its terminals. The maximum power dissipation of a single resistor is 0.25 W. Designing for half of the rated power results in the current conducted through the resistors being 2.786 mA according to Ohm's law. The resistance for each individual resistor is thus 16.1 kΩ. The resistance is chosen at 18 kΩ since it is a commonly used resistor value and the resistance lowers the current flowing through the resistors resulting in lower power dissipation.

6.2.2 Design of the damping components

The components placed around the voltage comparator help to stabilize it. The high gain of the comparator allows it to amplify its own noise as well as measured noise to such a degree that the comparator becomes unstable and begins to oscillate. The only viable method [25] of preventing the comparator from oscillating make use of capacitors and resistors to implement hysteresis and prevent noise from entering the comparator at its input terminals.

Capacitor C_1 with a suggested [25] value of 1 nF absorbs any high frequency noise before it enters the comparator. With less noise entering the comparator, there is less possibility of the comparator oscillating.

Resistor R_1 and R_3 implements hysteresis, which reduces the chance that the comparator may oscillate during the zero crossing of the tap voltage. The chosen value for resistor R_1 is 270 kΩ and for resistor R_2 is 1 MΩ respectively, as suggested in the data sheet of the LM311 [25].

6.2.3 Design of resistor R_6

The use of diodes D_1 and D_2 to clamp the voltage over the terminals of the voltage comparator has limitations. The diodes require a voltage over the terminals, which is larger than the forward voltage of the diode to allow the diode to conduct the current flowing through resistors R_4 and R_5. If the tap voltage over the diodes drops below the forward voltage of the diodes, these will stop conducting current and turn off. During this period when the tap voltage falls below the diode's forward voltage, the voltage over the terminals of the voltage comparator will float, which causes the comparator to oscillate. Placing resistor R_6 in parallel with the diodes allows the current flowing through resistors R_4 and R_5 to continue flowing, although the diodes are switched off.

The maximum voltage that the resistor will have over its terminals while conducting equals the forward voltage of the diodes of 0.95 V. The maximum current that will be conducted must be calculated. The minimum tap voltage to ensure that the diodes remain switched on is 0.95 V. The current flowing through either one of the diodes just before the diode stops conducting is 2.638 μA. The resulting resistance for R_6 results in 360 kΩ from Ohm's law.

6.2.4 Design of resistor R_2

The operation of the optical transmitter is controlled through the LM311. The LM311 switches the optical transmitter on by switching off the transistor inside itself and allows the current from the 5 V source to flow through the optical transmitter. Switching the optical transmitter off is accomplished by switching on the internal transistor of the LM311. The internal transistor of the LM311 has a lower on-state voltage than that of the optical transmitter,

and so the optical transmitter switches off with all the current flowing through the LM311.

Thus designing the resistance of R_2 to limit the current through the voltage comparator is just as crucial as allowing enough current to flow through the optical transmitter. The optical transmitter requires 60 mA of current to operate effectively, but the LM311 is capable of conducting only 50 mA of current. The result is that the resistance of R_2 must be calculated to take into account the currents that flow through both the LM311 and the optical transmitter. The saturation voltage of the transistor inside the LM311 is 0.75 V while the on-state voltage of the optical transmitter is 1.67 V. Calculating the resistance of R_2 using Ohm's law [14], means that the resistance must be either 85 Ω or 55 Ω for the voltage comparator and optical transmitter respectively. The final resistance value for R_2 is thus chosen to be 85 Ω due to the resistor limiting the current through the voltage comparator while providing sufficient current for the optical transmitter.

The power dissipation for the resistor is 212.5 mW which is near the 250 mW limit of a 1206 package surface mount resistor. Implementing two 169 Ω resistors in parallel provides a total of 500 mW power dissipation between the two resistors with a combined resistance of 84.5 Ω.

6.2.5 Design results for the sign detector

Table 6.2 shows the values of all the components used to implement the sign detector as designed herein.

Component	Value
Voltage comparator	LM311
R_1	270 kΩ
R_2	2x167 Ω in parallel
R_3	1 MΩ
R_4	10x18 kΩ in series
R_5	10x18 kΩ in series
R_6	360 kΩ
C_1	1 ηF
D_1 & D_2	ES1D

Table 6.2: Controller board components.

6.3 IGBT driver boards

The IGBT driver serves as an interface between the controller board and the IGBT, with each IGBT requiring its own individual driver board. Each driver board receives the gating signals from the controller board through the fibre optic cables that connect the boards. These isolate the controller board from the high voltages switched by the IGBTs.

The IGBT driver board also measures the on-state voltage over the collector-emitter terminals of the IGBT. Measuring the voltage over the IGBT while conducting allows the driver board to monitor the current flowing through the IGBT. High currents desaturate the IGBT, thereby raising the collector-emitter voltage higher than the saturation voltage of the IGBT. Measuring the collector-emitter voltage of the IGBT allows the IGBT driver to determine whether the IGBT is conducting more current than that for which it is rated.

Commercially available IGBT drivers switch off the IGBT and send a fault signal to the controller immediately after the collector-emitter voltage has risen above a set limit. These commercially produced drivers are specifically manufactured for use in DC-to-AC converters but are inadequate for use in the IGBT-based tap changer. The switching scheme of the tap changer must be maintained during any fault conditions with the duty cycle of the PWM set to 0%.

The drivers used in the tap changer must only *inform* the controller of a fault condition but, it must not turn off the IGBT. Sending the fault signal to the controller allows the controller to select which IGBTs must be switched off in accordance with the switching scheme while providing a free-wheeling path for the inductor current.

The basic layout of the IGBT driver [4] that is used to drive the IGBTs in the tap changer is illustrated in Figure 6.5.

The driver chip IC_1, used on the IGBT driver board to drive the IGBT is a Texas Instruments UCC37321 driver. It provides the voltage and current required by the IGBT to switch on and off. Using a 3 Ω for the gate resistor R_1, as suggested by Semikron in the data sheet for the 1 700 V IGBT [20], limits the current provided by the driver to the IGBT.

The fault measurement circuit implements a LM311 as the voltage comparator used for IC_2. The voltage comparator connects to the collector terminal of the IGBT through diode D_1. Using an Ixys DH20-18A diode to block the high voltages during the periods when the IGBT is switched off, but conducts current through resistor R_2 when the IGBT is switched on. The reference voltage V_{ref} provides the voltage comparator with the limit voltage that the collector-emitter voltage may reach. The voltage comparator activates the optical transmitter to inform the controller board that the collector-emitter voltage has reached the set limit.

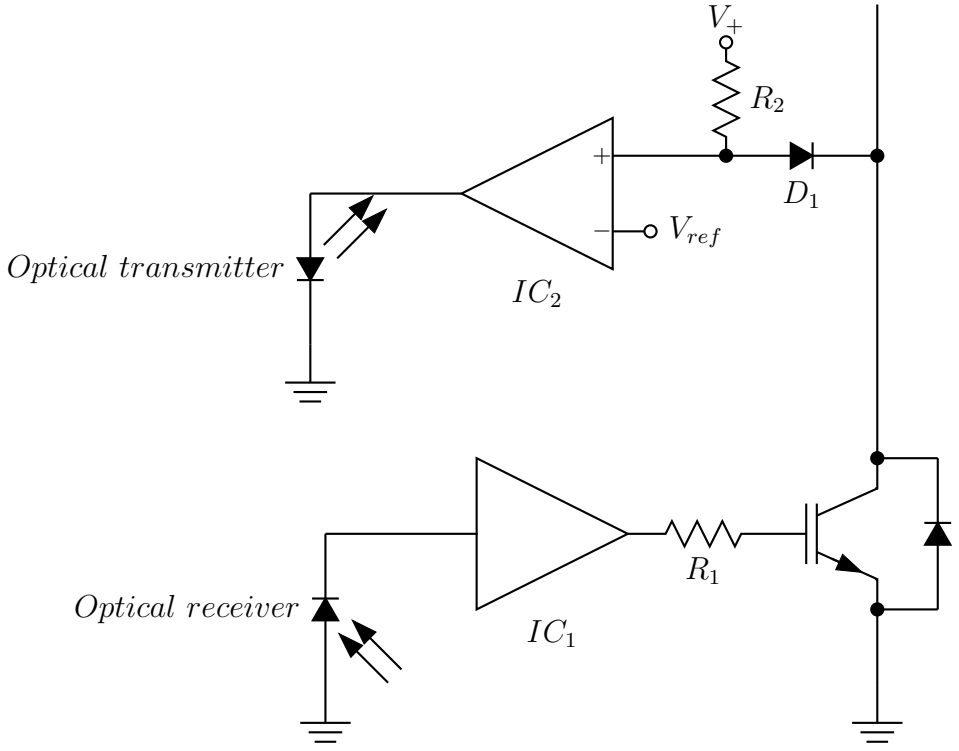

Figure 6.5: Basic layout [4] of the IGBT driver.

6.4 Bypass switch driver board

The circuit board that drives the bypass switch integrates two circuit boards into one in order to switch both thyristors S_1 and S_2. The circuit board provides the circuitry and components that are required to switch the thyristors for both over-voltage and over-current protection.

The basic layout of the circuit board used to drive the thyristor in the bypass switch is illustrated in Figure 6.6 [4] [26].

Table 6.3 below provides the values for the components used in the bypass switch.

Providing passive protection against over-voltages presents its own unique challenge. Making use of passive components to switch on the thyristors during over-voltage situations provides a failsafe method of performing over-voltage protection. Switching on the thyristors by means of a passive component layout requires the use of a break-over diode (BOD) [26] as indicated in Figure 6.6 [26].

A BOD only starts to conduct current after the voltage over the diode has reached the diode's break-over voltage. The current flowing through the BOD goes through the zener diode Z_2 and diode D_2 into the gate of the thyristor, turning on the thyristor. Diode D_1 [26] must be used in series with the BOD to block the high reverse voltages present over the thyristor since the BOD is

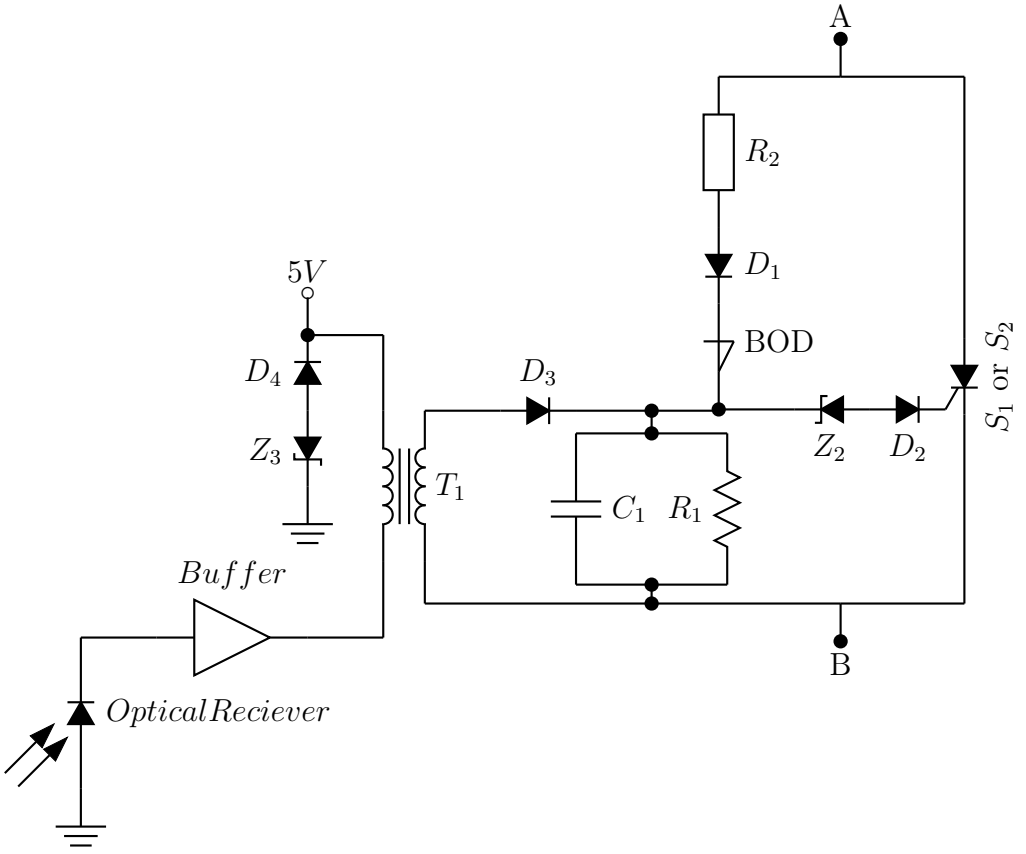

Figure 6.6: Basic circuit layout of the components used in the bypass switch driver board.

incapable of blocking reverse voltages larger than 10 V. Resistor R_2 limits the current that can flow through the BOD.

Resistor R_1 together with capacitor C_2 forms a snubber network [26] that prevents the thyristor from false triggering.

The over-current protection required to protect the IGBTs is implemented by also making use of the thyristors in the bypass switch. An over-current event takes place either when a fault signal has been generated by an IGBT driver, or when the load current measured by the controller has reached the specified limit. Pulsing the pulse transformer T_1 [4] through the optical receiver with a 20 kHz block-wave allows the controller to switch on the thyristors. Doing so just after the PWM has been deactivated forces the full load current through the thyristors.

6.5 Measurement board

Measuring voltage levels and current flow at specific locations in the tap changer allows the controller to respond accordingly to the measurements

Component	Value
Voltage comparator	LM311
R_1	500 Ω
R_2	100 Ω High voltage
C_1	47 nF
D_1 & BOD	Ixys IXBOD 1-14RD
D_2, D_3 and D_4	ES1D
S_1 and S_2	Semikron SKKT 720/22E thyristor
Optical receiver	Avago R-2521
Z_2	3 V Zener diode
Z_3	3.3 V Zener diode

Table 6.3: Bypass switch component values.

gathered. Responding to the measurements is vital, since non-response could seriously damage the tap changer.

The measurement board delivers two measurements to the controller, namely, the load voltage v_{Load} at the output of the tap changer and the load current i_O. Sending the load voltage to the controller allows the controller to set the duty cycle of the PWM accordingly in order to control the level of the load voltage. Measuring the load current merely serves as a protection mechanism, which is used to protect the IGBTs from over-current situations that may damage them.

Measuring the load voltage presents a challenge due to the high load voltage of 6 351 V. Many methods can be used to measure the load voltage, and each has its advantages and disadvantages. Measuring the load voltage by means of resistive division is a cheap yet effective method. But resistive division provides no isolation between the measurement board and the line voltage. Another implementation involves the use of a voltage transducer, which provides good isolation. However, it is an expensive component. The isolation provided by the voltage transducer makes it the ideal choice for use in the tap changer, and this is why it was used. The implementation of the voltage transducer is shown in Figure 6.7.

Measuring the load current is simply done with the use of a LEM current transducer. Figure 6.7 shows the implementation of the current transducer for use with the measurement board.

Both the voltage transducer and the current transducer deliver current outputs, which result in the use of resistors to convert the current into voltages that can be measured by an ADC. But the ADC implemented on the controller board is only capable of measuring voltages between 0 V and 5 V, with the advantage of providing a two's complement encoded output if the input voltage into the ADC centers around 2.5 V. Making use of opamps IC_1 and IC_2 shown in Figure 6.7 allows the measurement board to level shift the measured voltages

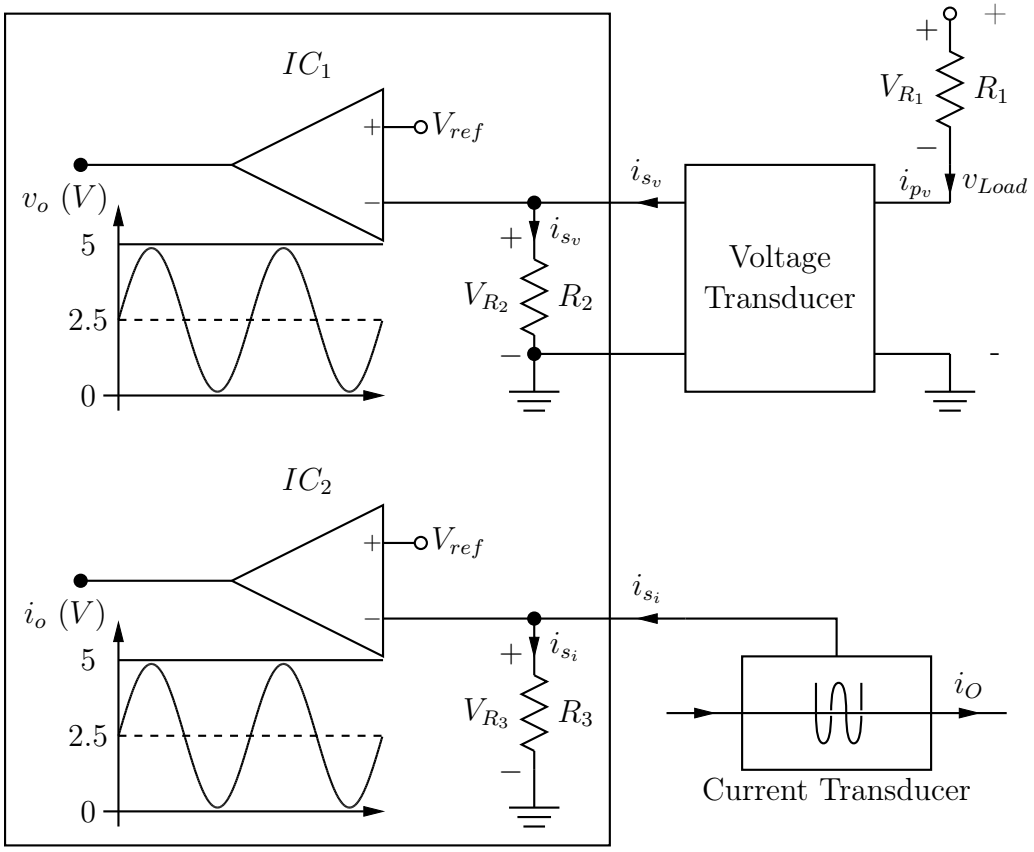

Figure 6.7: Basic circuit layout of the components used for the measurement board.

over the resistor to centre around any voltage with the use of the reference voltage V_{ref}. Setting V_{ref} to deliver an output voltage out of each opamp that centres around 2.5 V, results in the waveforms shown for each measurement in Figure 6.7.

The design of the resistors for use with either the voltage transducer or the current transducer is explained in the two following sections.

6.5.1 Load voltage measurement

The LEM voltage transducer that was chosen for measuring the load voltage v_{Load} is a LV 100-4000/SP12 [27] voltage transducer. It has a nominal measuring voltage of 4 000 V_{RMS} which is below the required nominal measuring voltage of 6 351 V_{RMS} and therefore requires the use of resistor R_1. Implementing R_1 in series with the voltage transducer forces the same current that flows through the primary of the transducer to flow through the resistor, resulting in a voltage drop over the resistor. Designing R_1 to have a voltage drop of 2 351 V_{RMS} over the resistor results in the voltage transducer measuring a voltage of 4 000V_{RMS}.

The peak terminal voltage of 5 656 V over the voltage transducer and the peak load voltage of 8 981 V result in a peak voltage drop of $V_{R_1} = 3\ 325$ V. The current flowing through the primary side i_{p_v} of the voltage transducer is 2.5 mA_{RMS}, creating a peak current of 3.536 mA. Using Ohm's law to calculate the required resistance for R_1 to force a voltage drop of 3 325 V over the resistor with the current at 3.536 mA results in R_1 being 940 kΩ.

The power dissipation of the resistor is 5.878 W; this necessitated the use of two 2 MΩ, 5 W resistors in parallel to form R_1.

The design of R_2 is based on the same principles as R_1. A peak design voltage of 2.45 V for V_{R_2} a peak output current $i_{s_v} = 70.71$ mA of the voltage transducer means that the resistance of R_2 must be 35 Ω. In view of the power dissipation of 86 mW, only a single 250 mW surface mount resistor is needed.

The resulting waveform of the measurement provided by the opamp to the ADC is shown by graph v_o in Figure 6.7.

6.5.2 Load current measurement

Using a LEM LF 205-S [28] current transducer allows the controller to measure nominal currents up to 200 A_{RMS}. Resistor R_3 converts the output current of current transducer into a voltage that can be level shifted by IC_2 before it is converted by the ADC. Designing resistor R_3 to convert the 141 mA peak current output i_{s_i} of the current transducer into a 2.45 V peak voltage results in a resistance of 17.37 Ω for R_3. The power dissipation required by the resistor is 173.7 mW, thus requiring two 33 Ω, 250 mW resistors in parallel to make provision for the power dissipation.

The resulting output provided by the opamp to the ADC is shown in the graph for i_o in Figure 6.7.

6.6 Summary

This chapter looked at the supporting hardware used in the IGBT-based tap changer. The main controller board featuring the FPGA and the supporting ICs for the FPGA were discussed. The sign detector board, which detects the polarity of the tap voltage over the IGBTs, was illustrated. The design of the IGBT-driver boards, which receive the gating signals from the FPGA via fibre optics to drive the IGBT, was presented. The driver circuit for the bypass switch, which implements a break-over diode for passive over-voltage protection, was reviewed. Lastly, the measurement board, which receives the voltage and current measurement from the respective transducers and scales the measured voltages for the controller board, was discussed.

Chapter 7

Voltage control design

Control of any device, be it electrical or mechanical is just as important as the device itself. The IGBT-based tap changer is no exception to this principle. One major purpose for which the IGBT-based tap changer has been designed is to regulate the output voltage delivered to the load. But regulating the load voltage requires a feedback control law to be added to into the IGBT-based tap changer in order regulate the voltage.

Figure 7.1 shows the components that make up the feedback controller that regulates the output voltage.

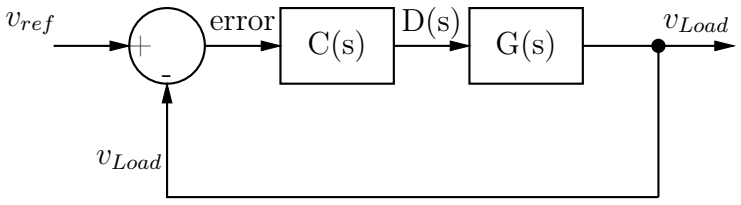

Figure 7.1: Symbolic layout of the feedback controller used in the tap changer.

Most of the components used to form the feedback controller are located inside the FPGA, with only the output voltage measurement performed outside the FPGA with the use of the ADC. The list below provides a brief description of each of the components mentioned in Figure 7.1.

- v_{ref}: The reference voltage input generated inside the FPGA uses a lookup table that provides the desired waveform and amplitude, which the output voltage v_{Load} must follow.
- v_{Load}: Digital representation of the load voltage measured with the ADC.
- Error signal: The error signal is the result of the load voltage v_{Load} subtracted from the reference voltage v_{ref}.

- Compensator C(s) block: The compensator takes the error signal and calculates the required duty cycle of the PWM to adjust the load voltage so that it follows the reference voltage.
- D(s) signal: Duty cycle set by the compensator for the PWM controlling the switching of the IGBT-based tap changer.
- Plant G(s) block: This block is the plant block, and it represents the transfer function of the tap changer in a mathematical format.

The design of the feedback controller is done by using the *Design by Emulation* [29] method as contained in the three steps below.

- Step 1: Determine the transfer function of the plant G(s), in this case the IGBT-based tap changer. The input of the plant model is the duty cycle while the output is the output voltage.
- Step 2: Design the compensator C(s) in the continuous time domain to compensate for the continuous plant model G(s) in order to control the output voltage delivered by the IGBT-based tap changer.
- Step 3: Digitize the compensator for implementation into the FPGA.

The implementation of these steps and the design of the required compensator to control the output voltage of the IGBT-based tap changer are described in the following sections.

7.1 Step1 : Determine IGBT-based tap changer plant G(s) model

The first step of deriving the continuous time domain transfer function of the plant for the IGBT-based tap changer involves simplifying the circuit diagram of the full system as set out in Figure 2.3 in Chapter 2. Since the IGBT-based tap changer consists of two synchronous buck converters, as already stated, it is possible for the IGBT-based tap changer to be simplified into a synchronous buck converter. Figure 7.2 shows the circuit diagram of a synchronous buck converter that was used herein for comparison, see the full system in Figure 2.3.

The ripple component of the inductor current i_{L_O} in Figure 7.2 flows to ground through capacitor C_O and returns to the inductor through whichever IGBT is switched on at that moment. The ripple component of the inductor current i_{L_O} in Figure 2.3 for the IGBT-based tap changer flows through capacitors C_1 or C_2 depending on which IGBT pair is switched on at the time before returning to the inductor. A comparison of the synchronous buck converter

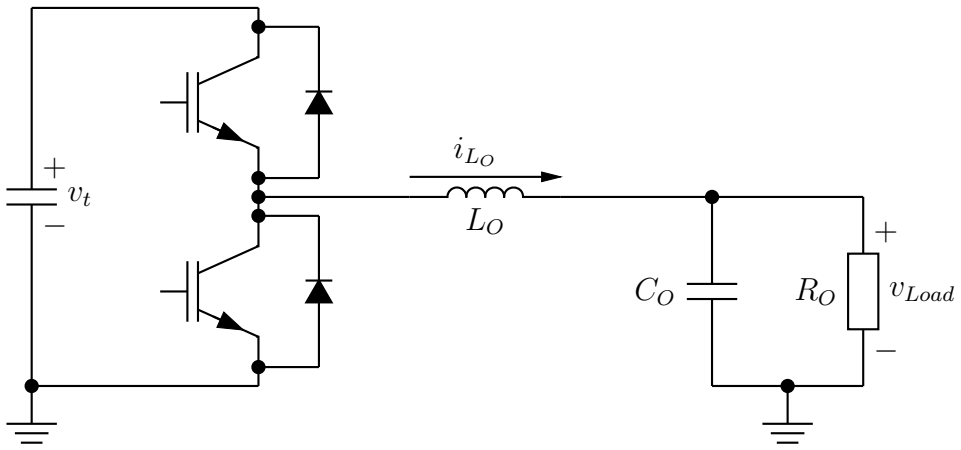

Figure 7.2: Synchronous bucking DC-to-DC converter.

and the IGBT-based tap changer reveals that the flow is the same and that it allows the IGBT-based tap changer to be simplified into the basic circuit layout as for a normal synchronous buck converter. The circuit diagram in Figure 7.3 therefore shows a simplified circuit diagram that was used to determine the transfer function for the IGBT-based tap changer. Capacitor C_1 and inductor L_1 represent the current flowing through the top tap of the transformer

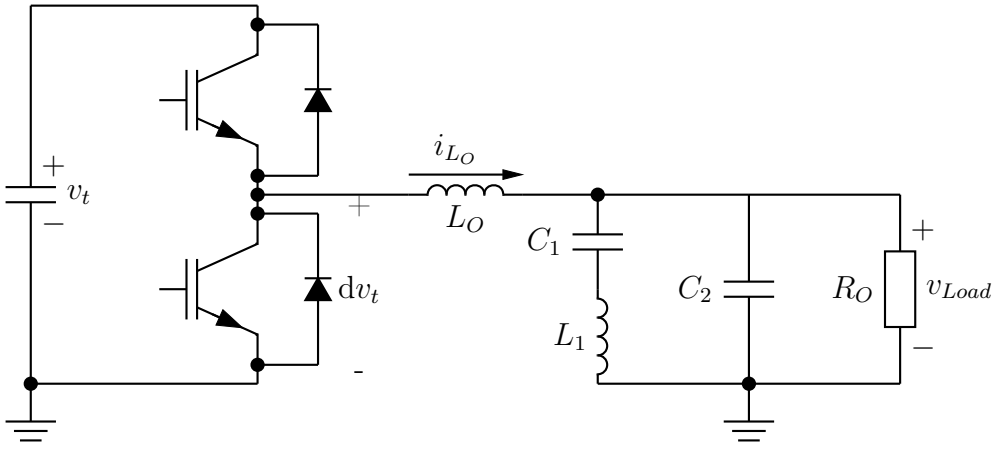

Figure 7.3: Simplified IGBT-based tap changer for the derivation of the transfer function.

The voltage applied to inductor L_1 depends on the duty cycle multiplied by the tap voltage v_t, which allows the transfer function to be determined with $\mathrm{d}v_t$ as the input and v_{Load} as the output. Redrawing Figure 7.3 into 7.4 includes only the components required for the calculation of the transfer function.

The circuit diagram in Figure 7.4 is similar to that in Figure 7.3 but with all the components rearranged and converted to the s-domain. The circuit diagram also contains the parasitic resistances of all the capacitors and inductors,

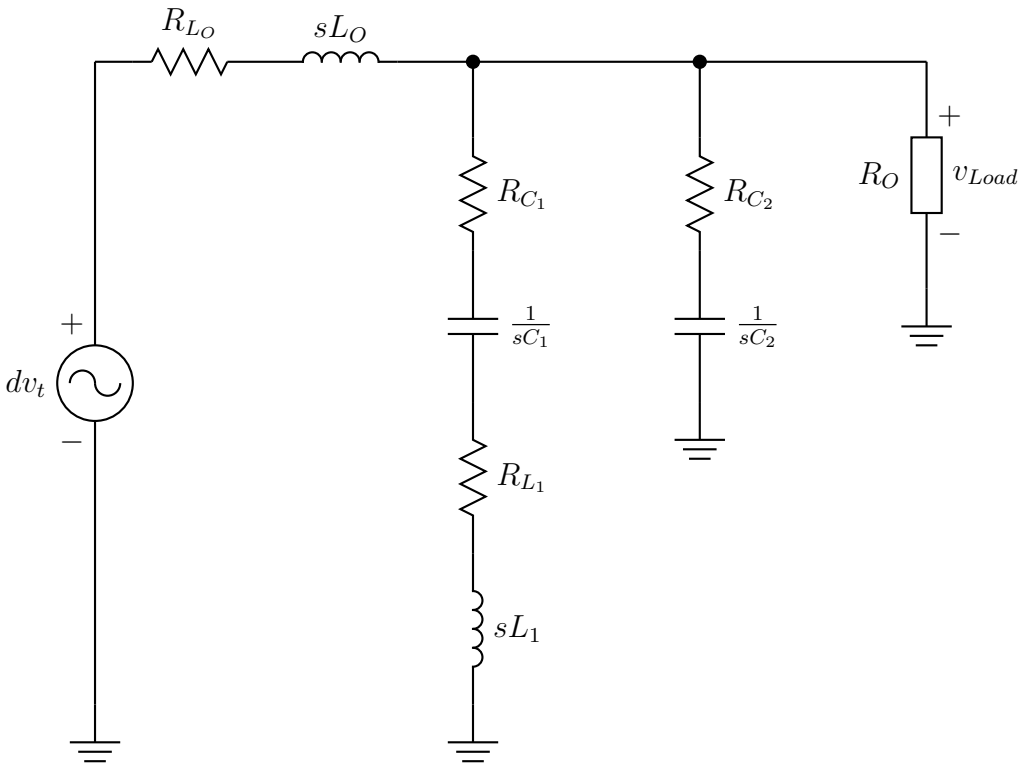

Figure 7.4: Simplified model used to derive the mathematical model from for the tap changer.

which represent the internal losses of the components that must be accounted for to ensure the accuracy of the transfer function.

The transfer function required for the plant requires the duty cycle d as the input and the load voltage v_{Load} as the output for the transfer function with the following form :

$$G(s) = \frac{V_{Load(s)}}{D(s)} \tag{7.1.1}$$

Deriving the mathematical model for the plant G(s) is based on Figure 7.4; the circuit diagram is simplified by adding the three parallel impedances into one single equivalent impedance. Calculating the parallel equivalent impedance by means of (7.1.2)[14] results in (7.1.3):

$$\frac{1}{Z_{eq}} = \frac{1}{R_O} + \frac{1}{R_{C_2} + \frac{1}{sC_2}} + \frac{1}{R_{C_1} + \frac{1}{sC_1} + R_{L_1} + sL_1} \tag{7.1.2}$$

$$\begin{aligned}
\frac{1}{Z_{eq}} &= \frac{\Big[R_O(\frac{1}{sC_2}+R_{C_2})+R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}) \\
&\quad +(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})\Big]}{R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})} \\
Z_{eq} &= \frac{R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})}{\Big[R_O(\frac{1}{sC_2}+R_{C_2})+R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}) \\
&\quad +(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})\Big]}
\end{aligned} \tag{7.1.3}$$

Using the single impedance value calculated in (7.1.3) simplifies the circuit diagram in Figure 7.4 into the circuit diagram shown below in Figure 7.5.

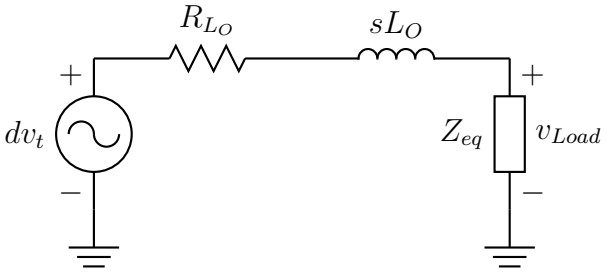

Figure 7.5: Further simplified model after the parallel impedances have been combined into one equivalent impedance.

Implementing voltage division [14] delivers the output voltage v_{Load} with reference to the input voltage dv_t shown in (7.1.4) below:

$$V_{Load}(s) = D(s)v_t\frac{R_{eq}}{sL_O+R_{L_O}+R_{eq}} \tag{7.1.4}$$

Substituting (7.1.3) into (7.1.4) delivers the transfer function of the plant G(s):

$$\begin{aligned}
\frac{V_{Load}(s)}{D(s)} &= \frac{v_t\left(\frac{R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})}{R_O(\frac{1}{sC_2}+R_{C_2})+R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})+(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})}\right)}{\left(\frac{R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})}{R_O(\frac{1}{sC_2}+R_{C_2})+R_O(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})+(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1})(\frac{1}{sC_2}+R_{C_2})}\right)} \\
&\quad +sL_O+R_{L_O}\Bigg)
\end{aligned} \tag{7.1.5}$$

Simplifying (7.1.5) by multiplying with (7.1.6) top and bottom :

$$R_O\left(\frac{1}{sC_2}+R_{C_2}\right)+R_O\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)$$
$$+\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)\left(\frac{1}{sC_2}+R_{C_2}\right) \tag{7.1.6}$$

Delivers (7.1.7) below:

$$\begin{aligned}\frac{V_{Load}(s)}{D(s)} &= \frac{v_t R_O\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)\left(\frac{1}{sC_2}+R_{C_2}\right)}{\left(sL_O+R_{L_O}\right)\Bigg[R_O\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)}\\ &\quad R_O\left(\frac{1}{sC_2}+R_{C_2}\right)+\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)\left(\frac{1}{sC_2}+R_{C_2}\right)\Bigg]\\ &\quad +R_O\left(\frac{1}{sC_1}+R_{C_1}+sL_1+R_{L_1}\right)\left(\frac{1}{sC_2}+R_{C_2}\right) \qquad (7.1.7)\end{aligned}$$

Simplifying (7.1.7) delivers the final transfer function of the plant G(s) in the continuous s-domain:

$$\frac{V_{Load}(s)}{D(s)} = v_t R_O \Bigg(\frac{1}{C_1 C_2} + s^3 L_1 R_{C_2} + s^2 \Bigg(R_{C_2} \Big(R_{C_2} + R_{L_1} \Big) + \frac{L_1}{C_2} \Bigg) + s \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) \Bigg)$$

$$\frac{}{s^4 \Big[L_O L_1 \Big(R_O + R_{C_2} \Big) \Big]}$$

$$+ s^3 \Bigg[L_1 \Big(R_O R_{C_2} + R_O R_{L_O} + R_{C_2} R_{L_O} \Big) + L_O \Big(R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_2} + R_O \Big(R_{C_1} + R_{L_1} + R_{C_2} \Big) \Big) \Bigg]$$

$$+ s^2 \Bigg[R_O \Bigg(L_O \frac{C_1 + C_2}{C_1 C_2} + R_{L_O} \Big(R_{C_1} + R_{L_1} + R_{C_2} \Big) + R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_1} \Bigg) + L_O \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) + R_{L_O} \Bigg(R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_1} \Bigg) \Bigg]$$

$$+ s \Bigg[R_O \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} + R_{L_O} \frac{C_1 + C_2}{C_1 C_2} \Bigg) + R_{L_O} \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) + \frac{L_O}{C_1 C_2} \Bigg]$$

$$+ \Bigg[\frac{R_O + R_{L_O}}{C_1 C_2} \Bigg] \tag{7.1.8}$$

Using the values provided in Table 7.1 for each of the variables used in the transfer function provides the solution to (7.1.8) used in Matlab.

The load resistance is taken at 5% of the full rated load resistance, resulting in a load resistance of 1 270.20 Ω

Figure 7.6 shows the result after performing a Bode analysis on the transfer function of the IGBT-based tap changer in MATLAB, including the values in Table 7.1.

Performing an AC transfer characteristic analysis on the model in Figure 7.4 in TINA (Texas Instruments Simulation software) delivers the Bode plot shown in Figure 7.7. Comparing the Bode plot of the mathematical model with the simulated Bode plot confirms the accuracy of the derived mathematical transfer function in (7.1.8). This can furthermore be confirmed by noticing

Variable description	Symbol	Value
Tap voltage	v_t	1 V
Series winding leakage inductance	L_1	202.159 μH
Output filter inductor inductance	L_O	265.66 μH
C_1 capacitance	C_1	88 μF
C_2 capacitance	C_2	88 μF
Load resistance	R_{Load}	1 270.20 Ω
L_1 parasitic resistance	R_{L_1}	0.635 1 Ω
L_O parasitic resistance	R_{L_O}	0.03 Ω
C_1 parasitic resistance	R_{C_1}	0.03 Ω
C_2 parasitic resistance	R_{C_2}	0.03 Ω

Table 7.1: Values for the constants used in the transfer function of the IGBT-based tap changer.

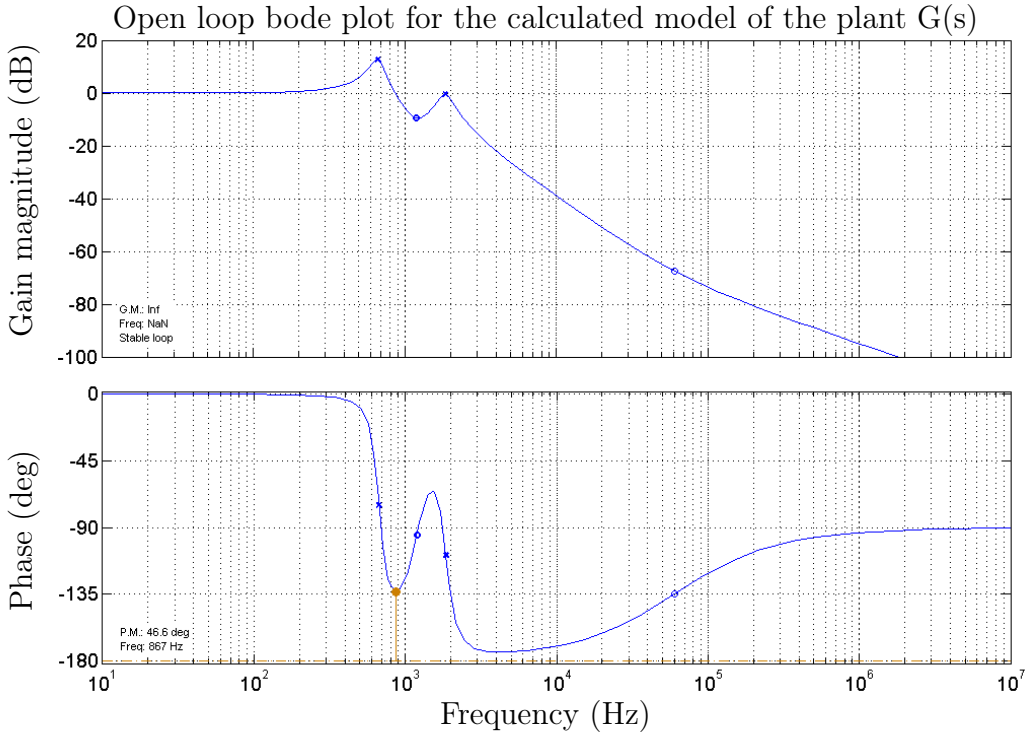

Figure 7.6: Bode plot of the open loop system for the calculated model.

the -3dB gain cut-off frequency on both plots at about 900 Hz and looking at the shape of the phase.

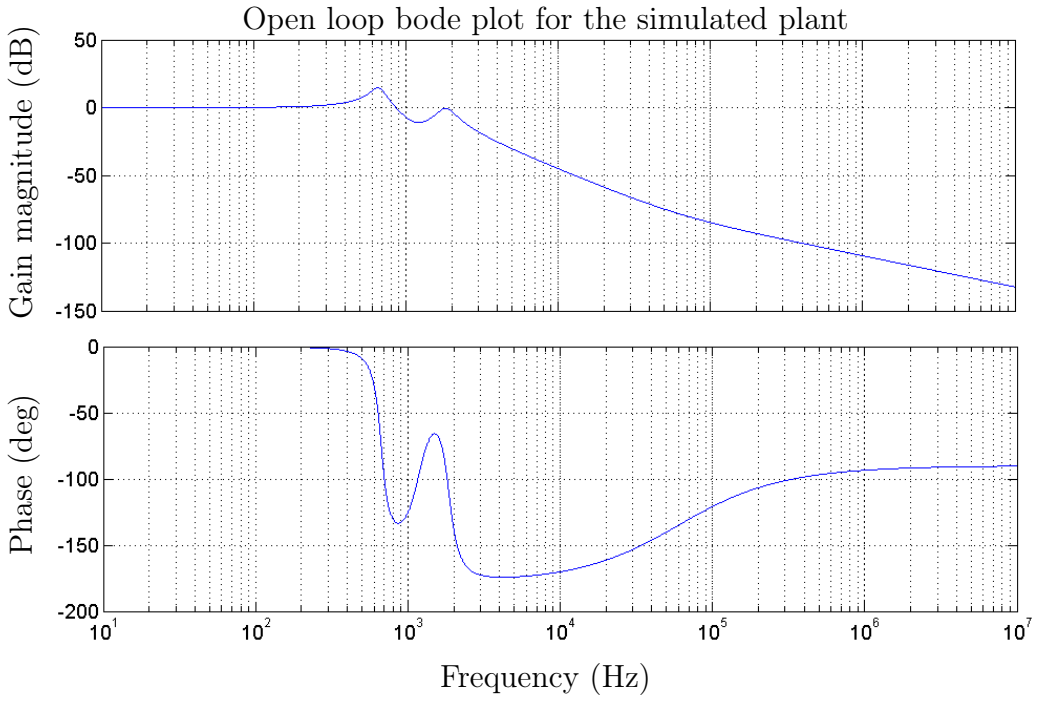

Figure 7.7: Bode plot for the system simulated with TINA.

7.2 Step 2: Compensator C(s) design

The most important component required to control the load voltage of the IGBT-based tap changer is the compensator. The compensator is designed according to the model of the plant presented in the previous section.

The design of the compensator starts with the selection of an appropriate compensator that works best for the specific plant G(s). The root locus of the plant, as illustrated in Figure 7.8, shows the position of the poles and zeros of the plant, which helps to determine which compensator should be used.

The root locus shows that the plant features two complex poles and one complex zero. It is suggested [30] that a proportional-integral derivative (PID) compensator [30] be implemented with a high frequency pole due to the presence of the complex poles. The PID controller in (7.2.1) [30] combines a complex zero and a pole; the zero is designed to counter the effect of the complex poles of the plant.

$$C(s) = G_{cp}\frac{s^2 + 2\zeta_{cp}\omega_{cp}s + \omega_{cp}^2}{s(s+\omega_p)} \tag{7.2.1}$$

The complex zero in the compensator is determined by the calculated natural frequency ω_{cp} for the zero, together with a specific damping ratio ζ_{cp}. The gain G_{cp} and the position of the pole ω_p make up the final elements of the compensator.

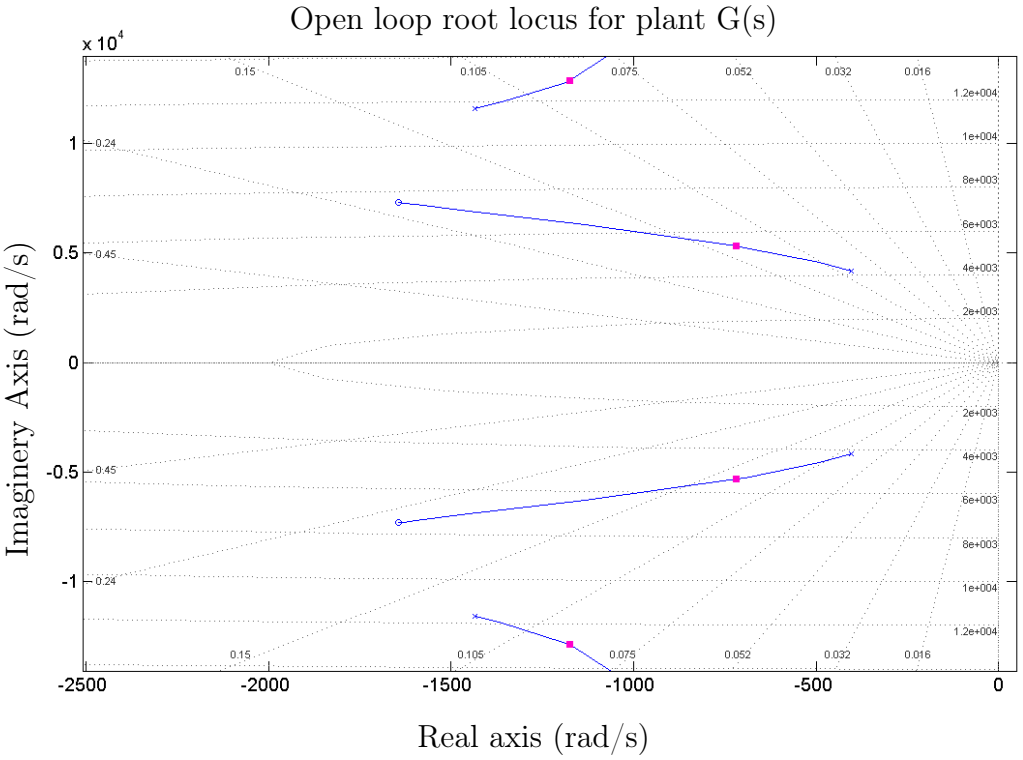

Figure 7.8: Root locus plot of the open loop system without compensation.

The main design specification for the compensator is to control the cut-off frequency of the IGBT-based tap changer to be $\omega_{0dB} = 6283$ rad/s. Designing for a cut-off frequency of 6283 rad/s allows the fundamental to pass through the compensator, while the high frequency switching is attenuated. The phase margin for the compensated plant is chosen at $\phi_M = 57.5°$, which is in the middle of the suggested [30] phase margin of between 45° and 70°.

The position of the complex zero in the compensator is designed to compensate for one of the complex poles of the plant. This means that one complex pole has to be chosen for which the compensator must compensate. The positions of the two poles are shown in (7.2.2) and (7.2.3) respectively.

$$s_1 = -402.8752\ 5 \pm j4\ 185.465\ rad/s \tag{7.2.2}$$

$$s_2 = -1\ 433.712 \pm j11\ 573\ rad/s \tag{7.2.3}$$

Using the natural frequency of each pole helps to determine which pole will be easier to compensate for, with the slower one being the ideal choice. Table 7.2 shows the natural frequency for each of the two poles together with their damping ratios.

Pole s_1 in (7.2.6) features the smaller natural frequency of the two poles, which is used for designing the complex zero. This design of the complex zero

Description	Symbol	Value
Natural frequency of pole s_1	ω_{n_1}	4 204.81 rad/s
Damping ratio for pole s_1	ζ_1	0.096 256
Natural frequency of pole s_2	ω_{n_2}	11 661.47 rad/s
Damping ratio for pole s_2	ζ_2	0.123 88

Table 7.2: Natural frequency and damping ratio for each of the two poles.

takes into account the natural frequency of the pole and the damping ratio. Designing the complex zero for a natural frequency 30 % smaller [30] than that of the pole results in $\omega_{cp} = 3\ 234.47$ rad/s. The damping ratio of the complex zero is designed to have a damping ratio twice than the damping ratio of the pole resulting in ζ_{cp} 0.192 511.

With the natural frequency and the damping ratio of the complex zero for the compensator now known, the pole of the compensator can be designed. This is done to correct the phase margin of the compensator so that the plant with the compensator has an additional feature of a specified phase margin of 57.5°. The design of the pole starts by calculating the required phase of the compensator by taking into account the phase of the converter and the required phase margin. Using (7.2.4) [30] together with the required phase margin of 57.5° and the converter phase ϕ_{cv} = -133.4° results in the compensator phase being $\phi_{cp} = 13.4°$.

$$\phi_{cp} = \phi_M - 180° - \phi_{cv} \tag{7.2.4}$$

Once the required compensator phase is known, (7.2.5) [30] can be used to calculate the multiplication factor.

$$f_{ct} = tan(90° + \frac{\phi_{cp}}{2}) \tag{7.2.5}$$

The multiplication factor is used together with (7.2.6) [30] to determine the final position of the pole.

$$\omega_p = \sqrt{\omega_{cp}\omega_{0dB}} f_{ct}^2 \tag{7.2.6}$$

Using (7.2.5) to calculate the multiplication factor results in a value of -8.513. If the natural frequency of the zero of the compensator is $\omega_{cp} = 3\ 234.47$ rad/s, while the specified cut-off frequency for the plant is $\omega_{0dB} = 6\ 283$ rad/s, this results in a pole position of $\omega_p = 326\ 668.86$ rad/s using (7.2.6).

The known values are used in (7.2.7) illustrating the values of the compensator. This means that only the gain is still unknown.

$$C(s) = G_{cp}\frac{s^2 + 1\ 245.34s + 10\ 461\ 800}{s(s + 326\ 668.86)} \tag{7.2.7}$$

Using the sisotool in Matlab allows the gain to be adjusted in real time until the required specifications for the compensated plant are reached. Using this tool results in a gain value of $G_{cp} = 37.553$; the Bode plot for this gain value is shown in Figure 7.9.

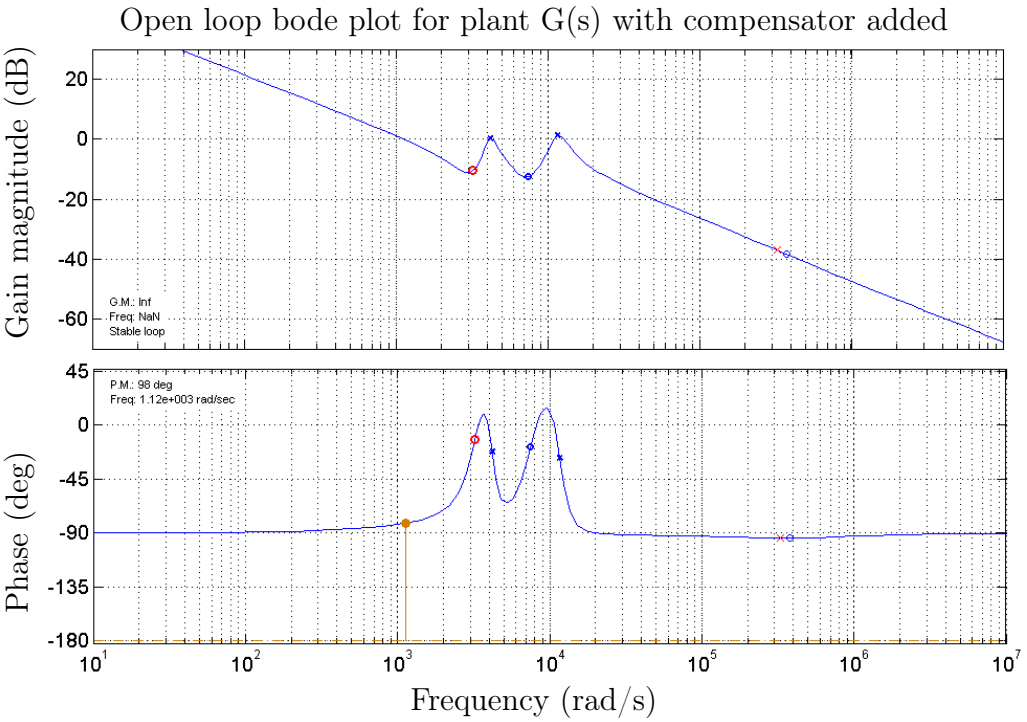

Figure 7.9: Bode plot of the compensated open loop system.

However, the Bode plot shows that the system does not comply with the specified phase margin at the required cut-off frequency. In order for the compensator to control the plant with the specified requirements, the pole of the compensator has to be moved until the required phase margin is achieved. Moving the pole in sisotool provides a quick trial and error method that can be used until the required phase margin is as close as possible to the required cut-off frequency. The resulting pole from this method is positioned at -3 095.8 rad/s, while the resulting gain is 1.275. The Bode plot for the final system is shown in Figure 7.10, while Figure 7.11 shows the final root locus of the plant with the compensator added.

The final compensator designed to control the IGBT-based tap changer is shown in (7.2.8), and it includes the redesigned gain and pole.

$$C(s) = 1.275\frac{s^2 + 1\ 245.34s + 10\ 461\ 800}{s(s + 3\ 095.8)} \tag{7.2.8}$$

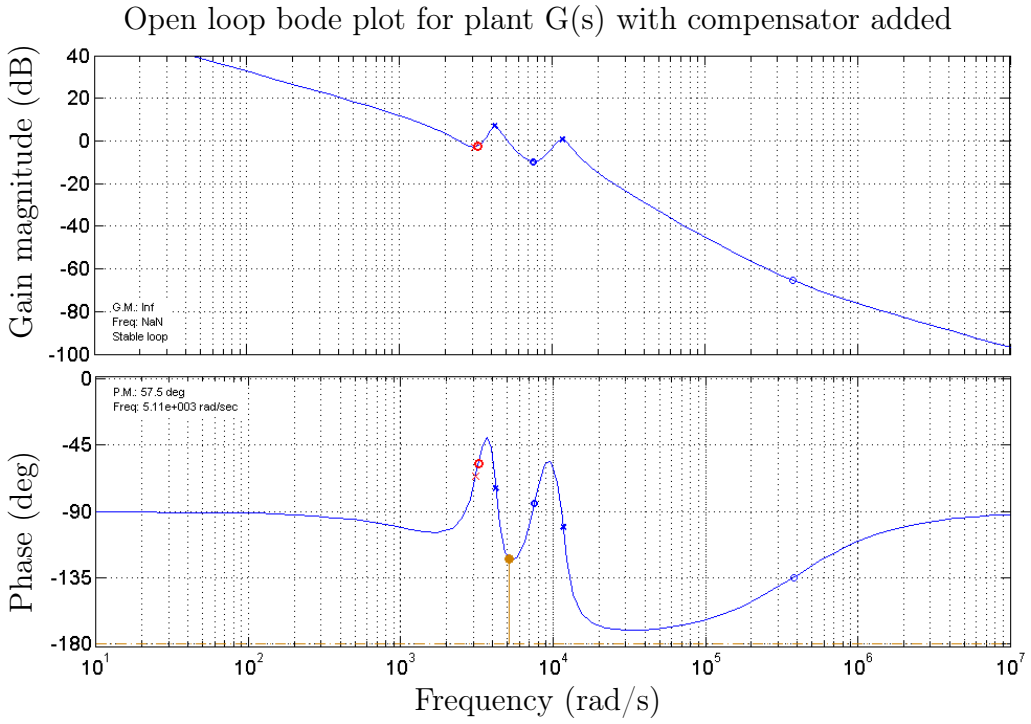

Figure 7.10: Bode plot of the compensated open loop system after the pole as been adjusted.

The final Bode plot in Figure 7.9 shows that the plant with the compensator added in (7.2.8) allows the fundamental to pass through, while the switching frequency of the converter is attenuated. The required phase margin for the system is also reached.

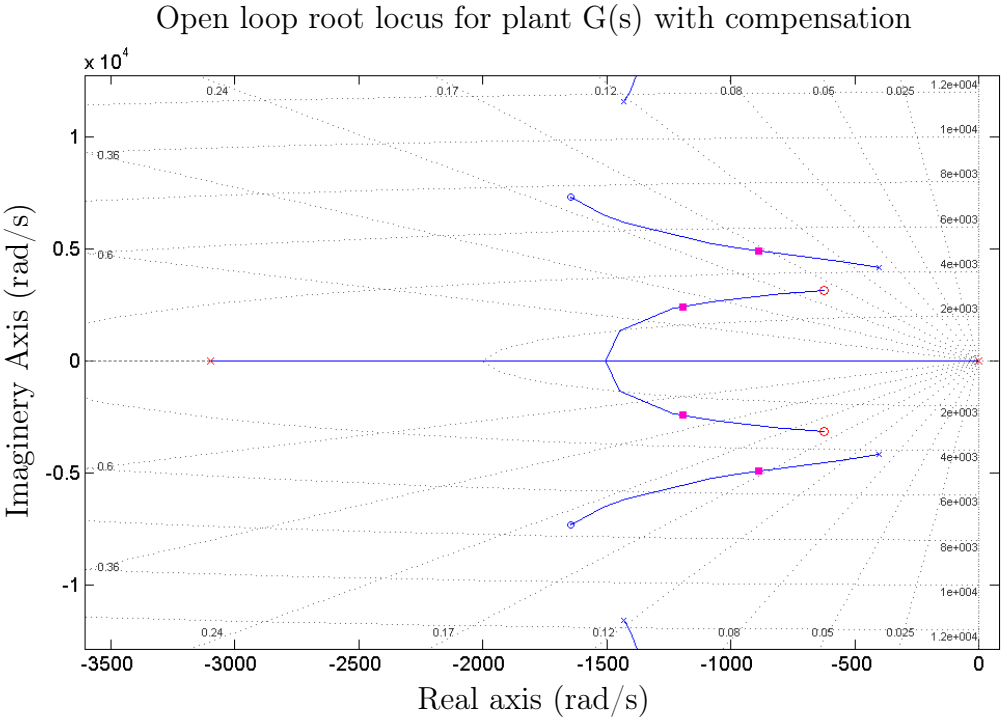

Figure 7.11: Root locus plot of the compensated open loop system.

7.3 Step 3 : Digitize the compensator

Once the design of the compensated system has been verified, the compensator must be transformed from the continuous s-domain to the discrete z-domain for implementation into a FPGA. Using Tustin's method [29] to digitize the continuous compensator by using the c2d command in Matlab with a sampling time of 0.000 1 seconds, results in (7.3.1) below:

$$C(z) = 1.202\frac{z^2 - 1.789z + 0.885\ 2}{z^2 - 1.732z + 0.731\ 9} \tag{7.3.1}$$

However, the discrete compensator in (7.3.1) cannot be implemented in a FPGA without rewriting it to make the implementation easier. Multiplying (7.3.1) with $\frac{z^{-2}}{z^{-2}}$ simplifies the equation by expressing the compensator so that it makes use of the previous samples for the calculations:

$$\begin{aligned} C(z) = \frac{Y(z)}{X(z)} &= 1.202\frac{1 - 1.789z^{-1} + 0.885\ 2z^{-2}}{1 - 1.732z^{-1} + 0.731\ 9z^{-2}} \\ Y(z)\Big(1 - 1.732z^{-1} + 0.731\ 9z^{-2}\Big) &= 1.202X(z)\Big(1 - 1.789z^{-1} + 0.885\ 2z^{-2}\Big) \\ Y(z) &= 1.202\Big(X(z) - 1.789X(z)z^{-1} \\ &\quad +0.885\ 2X(z)z^{-2}\Big) + 1.732Y(z)z^{-1} \\ &\quad -0.731\ 9Y(z)z^{-2} \end{aligned} \tag{7.3.2}$$

Rewriting Y(z) and X(z) to work with the specific sample k of Y(z) and X(z) makes use of the transformations in (7.3.3) below:

$$\begin{aligned} Y(z)z^{-2} = y(k-2) \qquad Y(z)z^{-1} = y(k-1) \qquad Y(z) = y(k) \\ X(z)z^{-2} = x(k-2) \qquad X(z)z^{-1} = x(k-1) \qquad X(z) = x(k) \end{aligned} \tag{7.3.3}$$

Substituting the values for Y(z) and X(z) of (7.3.3) into (7.3.2) and simplifying:

$$\begin{aligned} y(k) &= 1.202\Big(x(k) - 1.789x(k-1) + 0.885\ 2x(k-2)\Big) \\ &\quad +1.732y(k-1) - 0.731\ 9y(k-2) \end{aligned} \tag{7.3.4}$$

But with $y(k) = d(k)$ the output of the compensator and $x(k) = error(k)$ the input into the compensator delivers :

$$\begin{aligned} d(k) &= 1.202\Big(error(k) - 1.789error(k-1) + 0.885\ 2error(k-2)\Big) \\ &\quad +1.732d(k-1) - 0.731\ 9d(k-2) \end{aligned} \tag{7.3.5}$$

Due to the tap changer switching, an AC source requires the gain of the compensator to be changed continuously, as the tap voltage v_t changes. The gain of the compensator for a tap voltage v_t of 899 V is 0.001 326, while the gain for a tap voltage v_t of 1 V is 1.202. Because the gains are different, the compensator gain has to be dynamic. The simplest method of implementing such a dynamic gain structure is to set the compensator gain to 1.202, and then to divide it by the tap voltage. The result delivers the gain required by the compensator, depending on the tap voltage v_t. Adding the dynamic gain to (7.3.5) delivers the final compensator implemented into the FPGA with dynamic gain in (7.3.6) below.

$$\begin{aligned} d(k) &= \frac{1.202}{v_t}\Big(error(k) - 1.789error(k-1) + 0.885\ 2error(k-2)\Big) \\ &\quad +1.732d(k-1) - 0.731\ 9d(k-2) \end{aligned} \tag{7.3.6}$$

The tap voltage v_t used in (7.3.6) can either be measured or generated in the FPGA. Measuring the tap voltage presents some unique challenges with regard to the voltage levels at which the taps operate. Two methods can be used to measure the tap voltage; one connects a single voltage transducer directly over the taps, thus measuring v_t directly. The other method measures the top tap voltage and the bottom tap voltage separately, and then subtracts these values from each other in order, to arrive at the voltage between the taps. Both of these methods require an extra voltage transducer or two, making the IGBT-based tap changer more expensive to build.

However, if with the tap voltage is smaller than the input voltage and only 10% of the input, then a different approach can be used, utilizing only the FPGA. Using a sinusoidal waveform generator in the FPGA allows the FPGA to simulate the tap voltage and directly to use the value from the generator for the compensator. The only problem with this approach is the reduced accuracy, but at least this implementation is not excessively costly and it can be easily implemented. As a result, the method that involves the FPGA to simulate the tap voltage will be implemented first and thereafter it will be required to be tested to see whether it works before the direct voltage measurement method is implemented.

7.4 Summary

This chapter looked at the design of a compensator for the IGBT-based tap changer that can be used to control the output voltage provided by the tap changer to the load. The step was to derive the mathematical model of the plant G(s), which resembles the IGBT-based tap changer. Thereafter, the compensator, which would compensate for the specific plant, was designed. A proportional-integral derivative (PID) controller with a high-frequency pole was chosen for the compensator and then the required positions of the compensator pole and zero were determined. The compensator behavior was verified by means of a Bode diagram to indicate the response of the compensator. Discretization of the compensator for implementation into a FPGA followed the design of the compensator, which included dynamic gain to make provision for the AC input voltage.

Chapter 8

Simulation results

This chapter looks at the operation of the IGBT-based tap changer which was simulated with Simplorer V7.0 Student edition. Simulating the full system, as presented in Figure 2.3 of Chapter 2, provides an in-depth analysis of the operation of an IGBT-based tap changer. Looking at the flow of current through the semiconductors and the passive components as well as the voltages over these components makes it possible to determine whether the design is viable and whether it can be implemented in practice.

Figure 8.1 shows the circuit diagram for the circuit used in Simplorer with the values for each component given in Table 8.1.

The series winding of the autotransformer is represented by the dependent voltage source EC1. This voltage source is set to 10 % of the voltage measured by VM3. L2 represents the leakage inductance of the series winding of the autotransformer with value a of 202.159 μH used simulation purposes, as calculated in Chapter 5. Current source I1 represents the load, which conducts 100 A_{RMS} of current for the simulations. The simulation operates the IGBTs with a switching frequency of 10 kHz at a duty cycle of 50%, while allowing for dead time, which is also implemented in the equation blocks. The chapter starts by looking at the general operation of the IGBT-based tap changer and thereafter conducts a more in-depth analysis of the details.

8.1 General Operation simulations

This section looks at the simulation results of the input and output voltages and currents of the IGBT-based tap changer. Operating at full rated power, with zero phase shift between the input voltage and the input current, the output voltage I1.V is slightly out of phase with the input voltage VM1.V in Figure 8.2. The phase shift between the input voltage and the output voltage is the result of the line inductance simulated by L2 and the filter inductor L3.

Comparing the input current in Figure 8.3, as measured measured through L2, and output current I1.A in Figure 8.4, shows that there is no phase shift

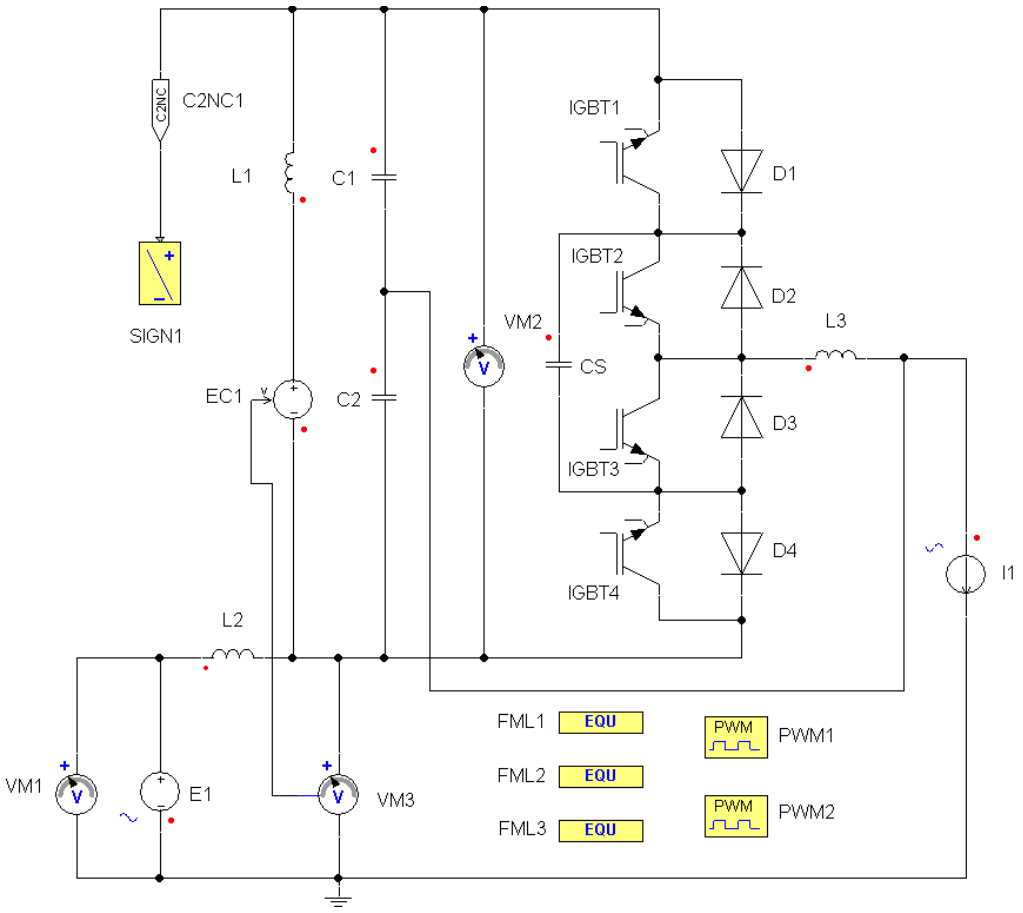

Figure 8.1: Circuit diagram of the full system used in Simplorer.

Description	Symbol	Value
Main input voltage	E1	6 351 V_{RMS}
Tap voltage	EC1	10 % of E1
Line inductance	L2	19.04 mH
Transformer series winding leakage inductance	L1	202.159 μH
Filter capacitors	C1 and C2	88 μF
Snubber capacitor	CS	116 μF
Output filter inductor	L3	266.65μH
Output current source	I1	100 A_{RMS}

Table 8.1: Values of the components used in Simplorer.

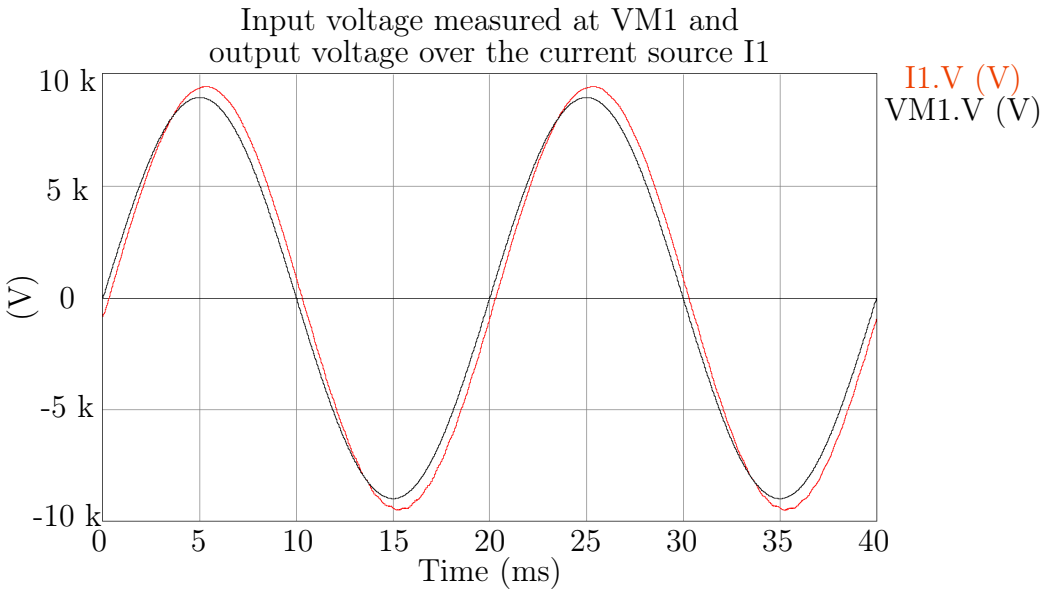

Figure 8.2: Input voltage and output voltage plotted together, showing a few degrees phase shift between the two.

between these two.

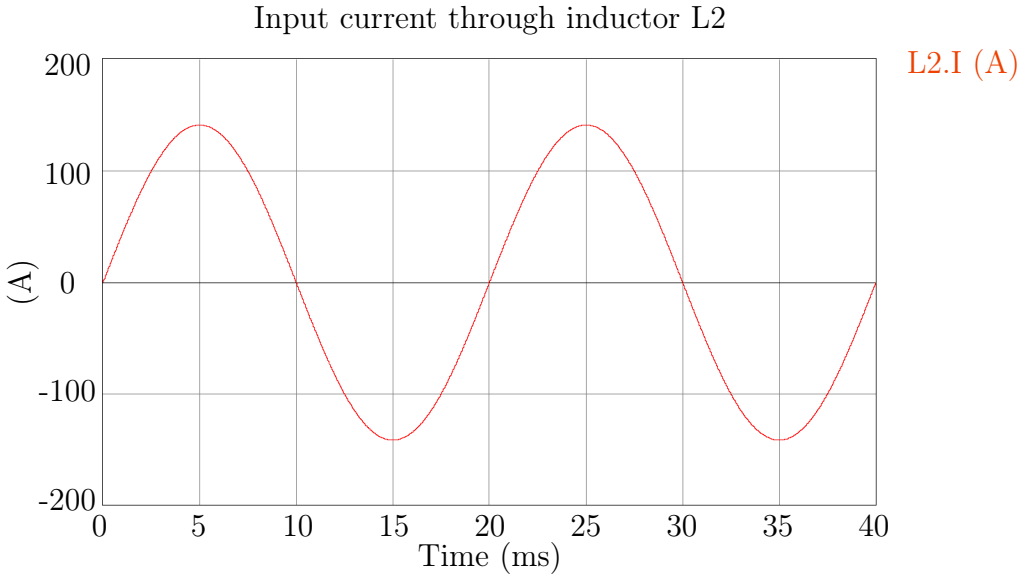

Figure 8.3: Input current delivered by voltage source E1 through the line inductance L2.

Phase shifting the output current so that is lags by 30° in Figure 8.5 shows that the IGBT-based tap changer always provides a current path while operating.

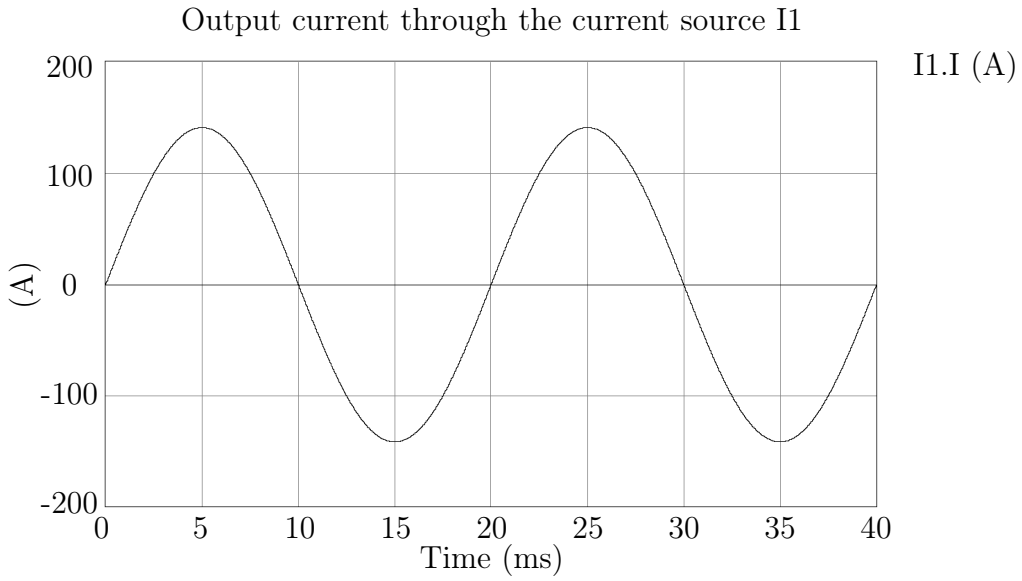

Figure 8.4: Output current delivered by the IGBT-based tap changer to the current source.

The same holds for a leading phase shift of 30° in Figure 8.6.

The ripple at the start of the plots in Figures 8.5 and 8.6 is due to the startup of the IGBT-based tap changer with zero initial currents. This effect dissipates after the first cycle of the fundamental has passed. The current I1.A is scaled by a factor of 10 for illustration purposes.

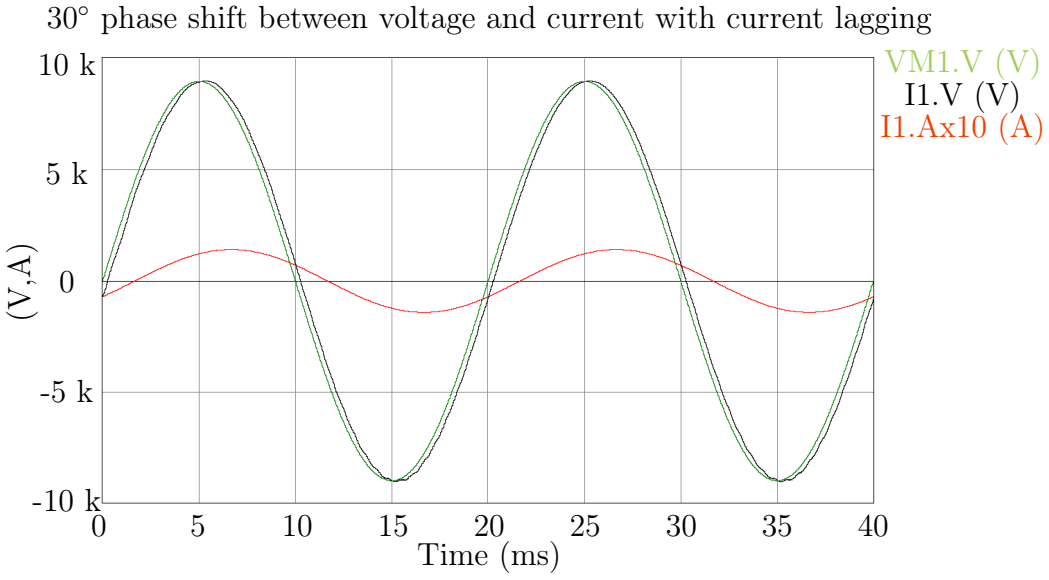

Figure 8.5: Phase shift between voltage and current with the current lagging the voltage.

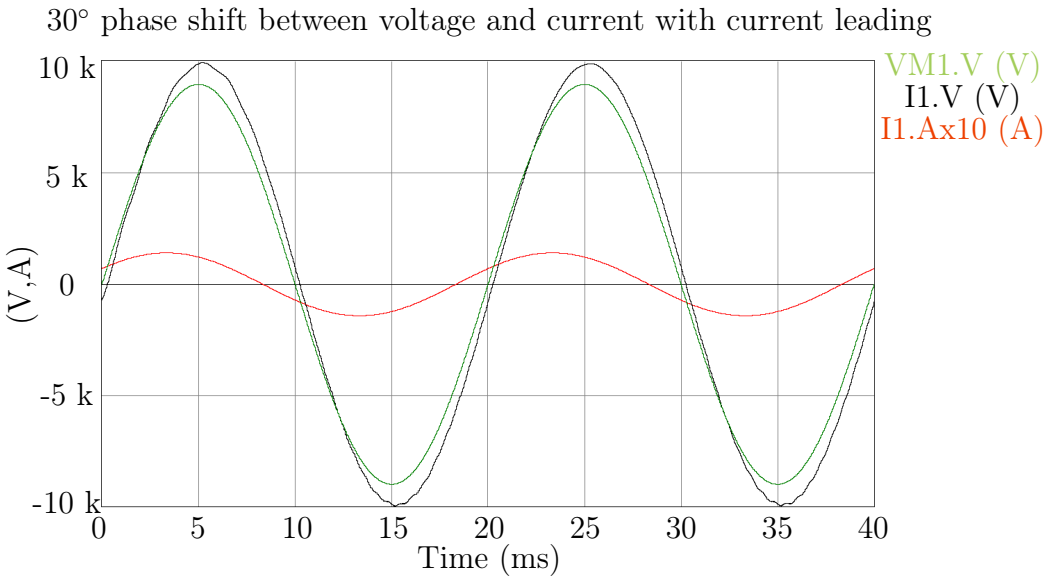

Figure 8.6: Phase shift between voltage and current with the current leading the voltage.

The ripple component present on the output voltage during the negative half cycle in all the graphs is due to the switching scheme. It is during this cycle that the snubber capacitor CS is shorted out and all the filtering is done by capacitors C1 and C2 alone. This is not present during the positive half cycle of the voltage, when the snubber capacitor CS is connected in parallel with capacitor C1 and C2, which are also operating as a filter.

The ripple during the negative cycle indicates that capacitors C1 and C2 are not able to filter the output voltage, and this requires the design to be fine-tuned to ensure better results before practical implementation.

The next section looks at the simulation of the switching scheme.

8.2 Switching scheme

The switching scheme presented in Chapter 2 depends on the polarity of the voltage over the IGBTs. A sign detector circuit provides a signal for the controller so that is knows exactly what the polarity of the voltage is. Using a sign block in Simplorer provides the same signal as the sign detector circuit board would in the practical implementation. Figure 8.7 shows the operation of the switching scheme, as the voltage over the IGBTs changes polarity.

The output of the sign block used in Simplorer is shown at the bottom of the graph, with a positive output value for positive polarity and a negative output for negative polarity in respect of the voltage over the IGBTs. The influence of the sign signal on the IGBT gating signals is shown in the waveforms at the top of the graph. It shows that IGBTs 1 and 4 are switched on

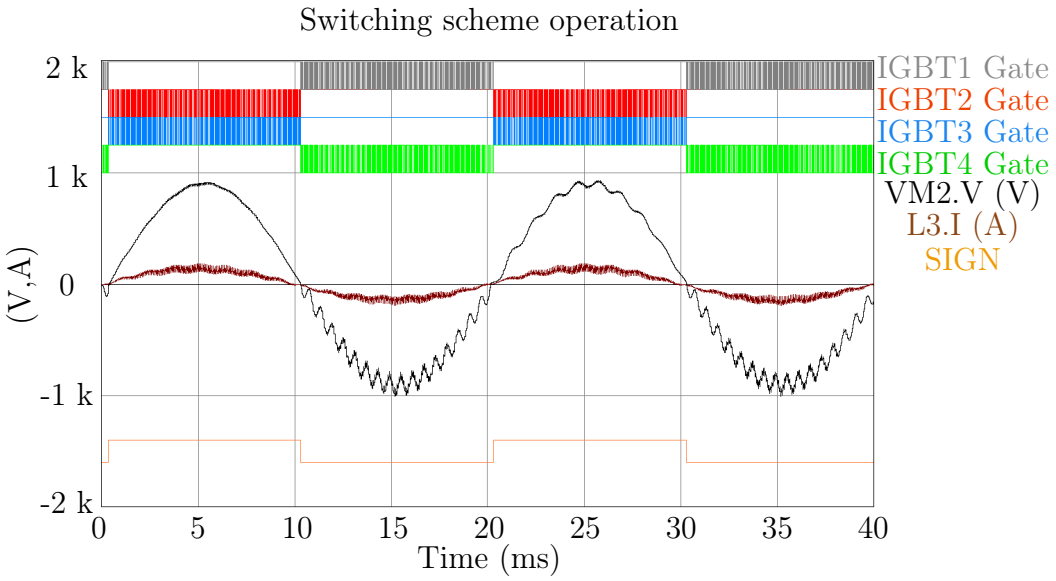

Figure 8.7: Waveforms showing the operation of the switching scheme with the gating signals for the IGBTs at the top. The voltage over the IGBTs and the current through the output filter inductor L3 are in the middle and the output of the sign detector is at the bottom.

permanently, while IGBTs 2 and 3 are pulse width modulated during positive voltage over the IGBTs; the reverse applies for negative voltage over the IGBTs. This is necessary for the correct operation of the IGBT-based tap changer, as described in Chapter 2.

The effect of the commutation is largest on the snubber capacitor, as already indicated in the previous section. Figure 8.8 shows how the snubber capacitor only filters the tap voltage during the positive half cycle of the tap voltage.

Looking at the operation of the IGBTs in the next section provides some insight into how the output voltage and current are provided by the IGBT-based tap changer.

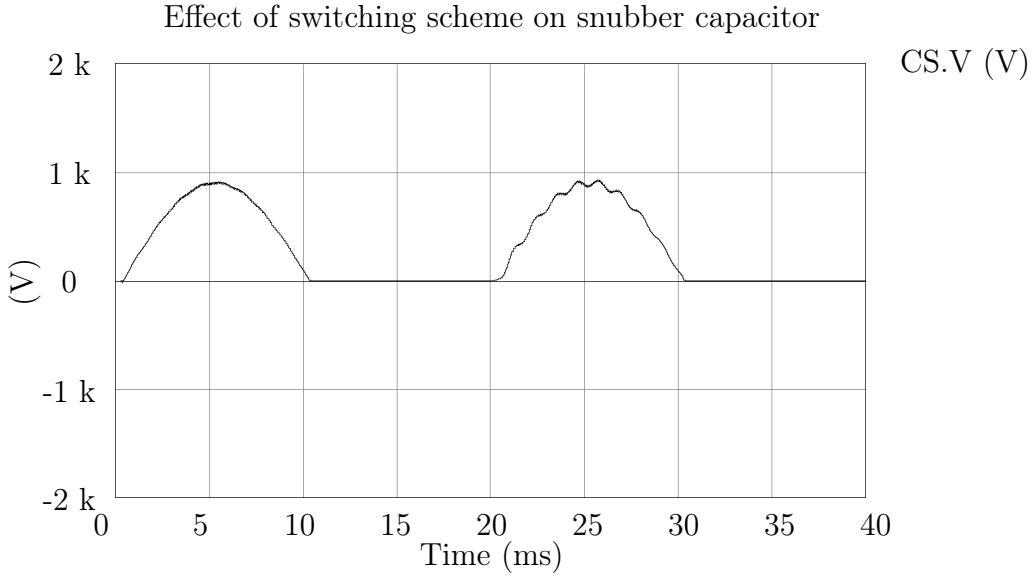

Figure 8.8: Waveform of the snubber capacitor voltage showing the influence of the commutation on the voltage over the capacitor.

8.3 Voltage over and current through the IGBTs

The switching scheme that is used to operate the IGBT-based tap changer forces the entire tap voltage over the pair of IGBTs, which are switched at high frequency. This also forces the pair of IGBTs that is switching at high frequency to conduct the full inductor current. Figure 8.9 shows the tap voltage measured by VM2 and the inductor current flowing through inductor L3, which is centred around the output current of current source I1. These voltages and currents are used as a reference for the next figure.

Figure 8.10 shows the voltages over IGBTs 2 and 3 while operating together with the current through IGBT2 and diode D3. The graph also shows the gating signals of IGBT2 and IGBT3 at the top of the graph.

The simulation of the inductor and the output current provides an ideal situation for verifying the inductance of the inductor. When the peak value of the ripple component of the inductor current is 182 A, while the peak output current is 141 A, this results in ripple component that is 22.5% of the output current. However, this value is within the design specification of up to 30%.

The black waveform shows the voltage over IGBT2, while the red waveform shows the voltage over IGBT3. It can clearly be seen that IGBT2 is switched off during the period when the voltage over the IGBT equals the tap voltage, as measured by VM2 in Figure 8.9. The same holds for IGBT3, which is switched off during the period when the voltage over the IGBT equals the tap voltage. But the off-state voltage over IGBT2 is a little higher than the

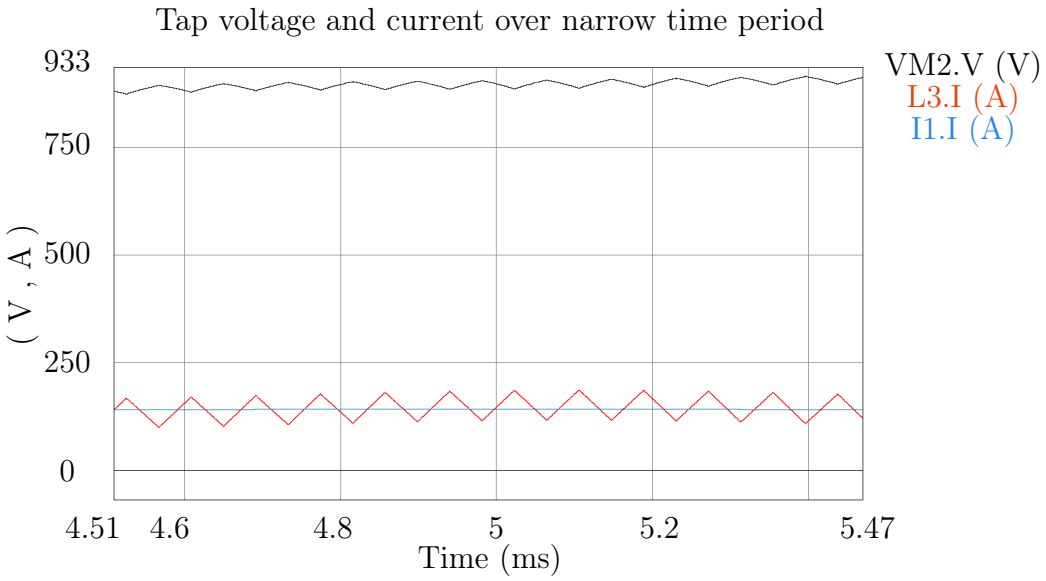

Figure 8.9: Voltage over the taps of the autotransformer together with the current flowing through the output inductor L3.

voltage over IGBT3, which can be attributed to the lower on-state voltage of diode D3 while it is conducting.

The voltage over IGBT2 stays positive while it is conducting the inductor current, which proves that IGBT2 is conducting the inductor current. This is not true for IGBT3, however: the voltage over IGBT3 drops below zero, indicating that diode D3 is conducting the inductor current because of the positive inductor current.

The inductor current L3 is thus conducted by IGBT2 and diode D3, as determined by the switching scheme: the inductor current rises while IGBT2 is switched on, and it falls while diode D3 conducts. This raising and lowering of the inductor current is due to the voltage over the inductor. The output voltage of the IGBT-based tap changer over the current source has a peak voltage of 9 412 V because 50% of the tap voltage is added to the input voltage. Thus, connecting the input into the inductor to the top tap will result in a positive voltage difference over the inductor causing the inductor current to rise. The reverse applies with connecting the inductor to the bottom tap, with the bottom tap voltage lower than the output voltage, which causes the inductor current to fall.

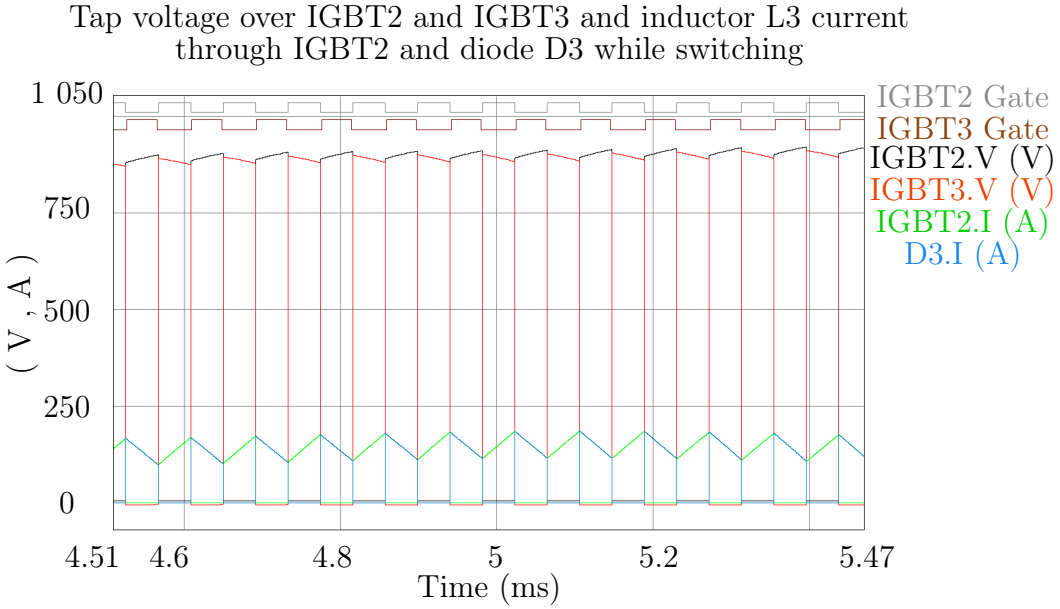

Figure 8.10: IGBT2 voltage, current and gating signal as well as IGBT3 voltage and gating signal with diode D3 current.

8.4 IGBT switch on and off simulation

Switching the IGBTs on and off, changes the voltage and current over and through the IGBTs as well as the diodes. When IGBT2 is switched on, it causes the voltage over this IGBT to fall, while current through is rises. The reverse occurs in the case of diode D3: the diode voltage increases, as the current through the diode falls. The rates at which the voltage and current exchanges occur between IGBT2 and diode D3 are equal, as shown in Figure 8.11.

The top two waveforms show the gating signals for IGBT2 and IGBT3. The effect of the dead time implemented into the PWM is clearly noticeable, as the gating signal for IGBT3 is low long before the gating signal for IGBT2 is applied. The voltage and current exchange only takes place at the instant when IGBT2 is switched on, while nothing happens when the gating signal for IGBT3 is removed.

In Figure 8.12, switching IGBT2 results in the voltage and current exchanging from IGBT2 to diode D3, while the gating signal to IGBT2 is being removed. IGBT3 is only switched on after the dead time period has elapsed, but this is not shown on the graph.

This current exchange between IGBT2 and diode D3 only applies in the case of positive inductor current and positive tap voltage; the voltage and current exchange is completely different in the case of negative inductor current. The voltage and current exchange with regard to negative inductor current takes place between IGBT3 and diode D2, depending on the gating signal

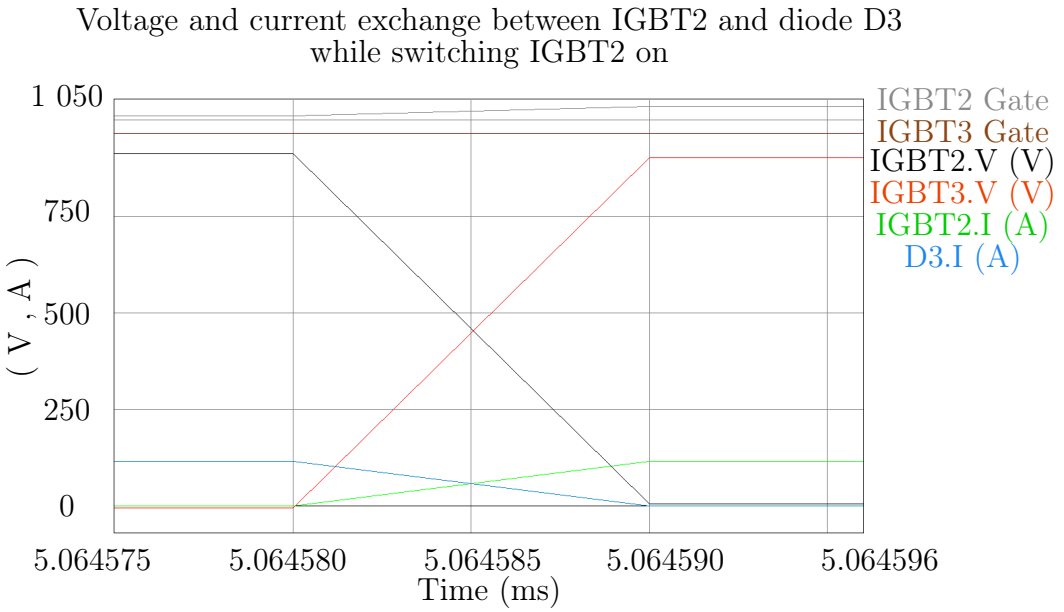

Figure 8.11: Switch-on behavior of IGBT2 while applying the gating signal to IGBT2.

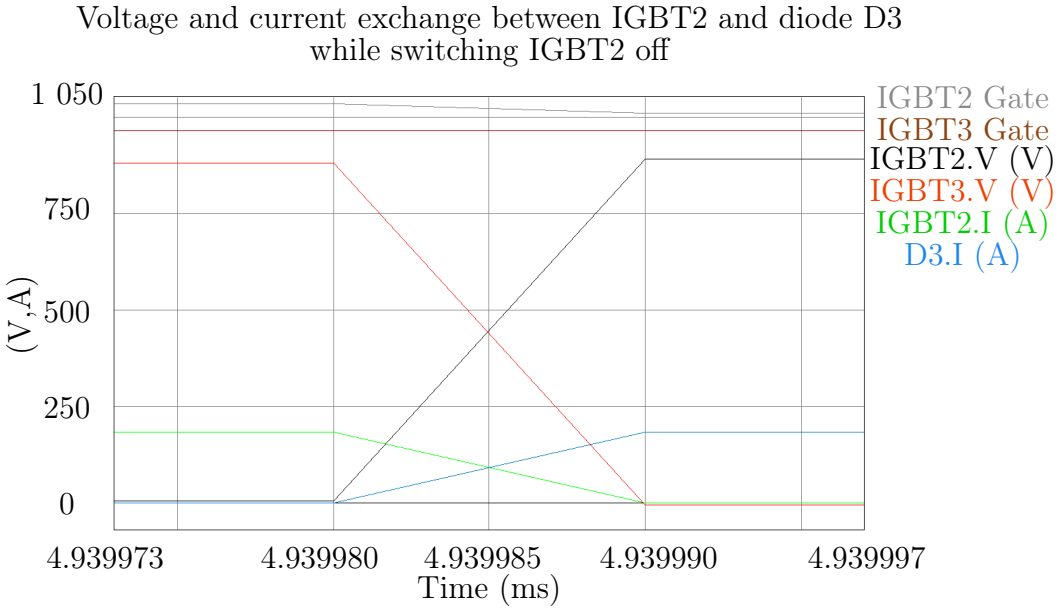

Figure 8.12: Switch-off behavior of IGBT2 while removing the gating signal from IGBT2.

applied to IGBT3. The results for negative inductor current are not shown, however, because the voltage and current exchange behaviour between the components is similar for negative inductor current.

8.5 Filter capacitor simulation

The influence of the passive components on the operation of the IGBT-based tap changer can clearly be seen in Figure 8.13. The graph shows the gating signals applied to IGBT2 and IGBT3 at the top of the graph, while the tap voltage measured by VM2 (red) shows that the simulation is analysed at the peak tap voltage.

The voltages over capacitors C1 and C2 shown in the middle of the graph show that the output voltage is half of the tap voltage, due to the 50 % duty cycle of the PWM. This can be attributed to the fact that the voltage over both capacitors is half the tap voltage; added together, they make up the tap voltage. Changing the duty cycle changes the voltage over these capacitors, which results in a higher voltage over one capacitor and a lower voltage over the other, but the sum of the two still equals the tap voltage. The result of changing the duty cycle is shown in Figure 8.14, with the duty cycle set to 75 %.

A closer look at the current flowing through the filter capacitors C1 and C2 as well as through the snubber capacitor CS shows that these currents equal the ripple current flowing through inductor L3. The ripple component of the inductor current is split between the capacitors, thus providing a return path for the ripple current of the inductor current. The benefit of this return path is that the ripple component of the inductor current does not go through the system, which therefore does not subject the load to any harmonics generated by the IGBT-based tap changer.

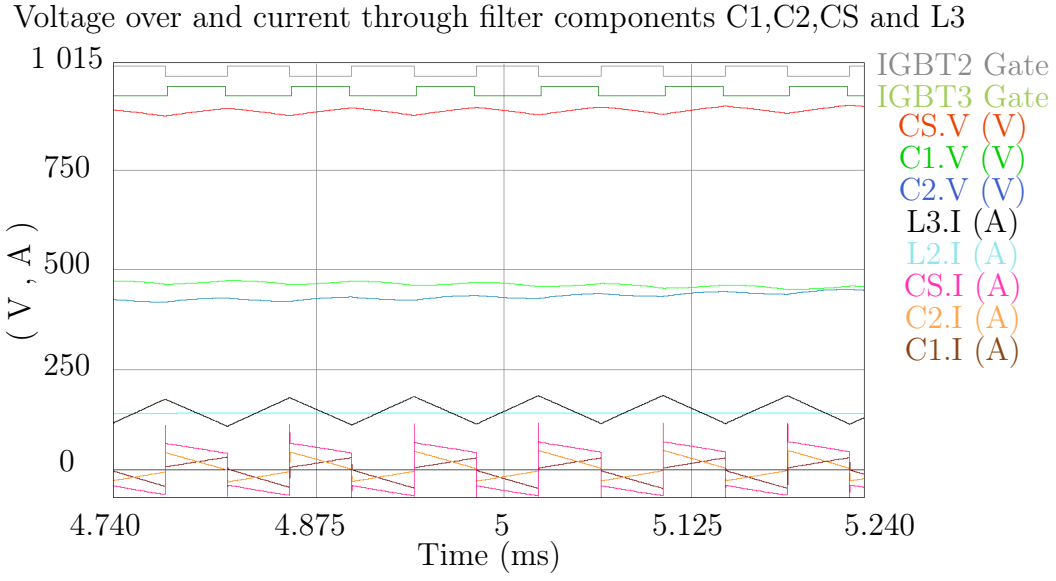

Figure 8.13: Graph showing the capacitor voltages and currents together with the gating signals for IGBT2 and IGBT3 for a duty cycle of 50 %.

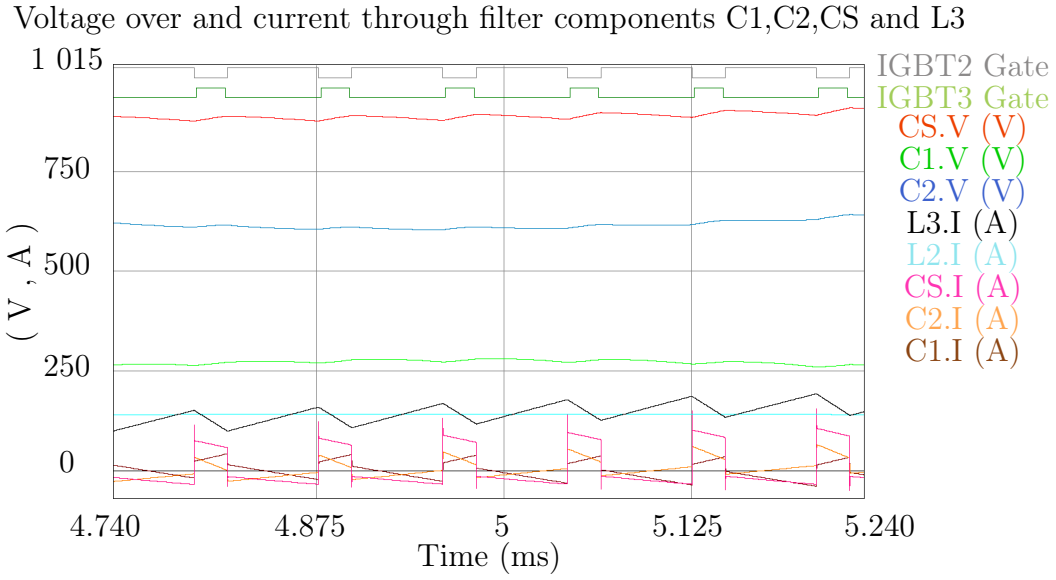

Figure 8.14: Graph showing the capacitor voltages and currents together with the gating signals for IGBT2 and IGBT3 for a duty cycle of 75 %.

8.6 Summary

This chapter has looked at the simulation results performed with Simplorer, focusing specifically on the influences of the different components on each other, while the IGBT-based tap changer was operating at rated power. The chapter began by discussing the input and output voltage waveforms, which showed that the output voltage lagged behind the input voltage by a few degrees. The simulation also showed the influence of the switching scheme on the operation of the snubber capacitor during the negative half cycle of the tap voltage.

Looking at the simulation of the behavior of the IGBTs showed that the IGBTs switch the full tap voltage on and off while operating and while they are conducting the full inductor current. It emerged from simulating the switch-on and -off behavior of the IGBT, that the inductor current tap voltage is conducted by one IGBT and one diode, while the IGBT-based tap changer switches at high frequency. The final simulation looked at the influence of the passive components on the IGBT-based tap changer. It was found that the tap voltage is split between the filter capacitors while the capacitors are conducting the ripple component of the inductor current.

Chapter 9

Practical measurement results

This chapter looks at the measurements gathered from the scale-model IGBT-based tap changer, which was built to verify the design of the tap changer. The chapter starts by presenting the layout of the scale IGBT-based tap changer and the ratings of the tap changer. This is followed by a discussion of the practical measurements, which were conducted on the scale-model IGBT-based tap changer in order to evaluate its operation and to verify the practicality of the design. An efficiency analysis of the scale-model IGBT-based tap changer is conducted. Lastly, the chapter accesses the design of the controller for the scale-model IGBT-based tap changer and the voltage regulation measurements.

9.1 Layout and ratings of the scale-model IGBT-based tap changer

An existing prototype (referred to as the scale-model IGBT-based tap changer) was used to test and verify the concept of IGBT-based tap changer as presented in this thesis. The software for the FPGA, however, was designed during the course of this thesis, and it is discussed in detail in Chapter 10. The layout shown in Figure 9.1, which was used to construct the scale-model, is the same layout as proposed for the IGBT-based tap changer.

The rating of the entire system is shown below in Table 9.1.

Description	**Value**
Power rating	5 kVA
Input voltage	212 V
Output voltage	230 V
Switching frequency	10 kHz

Table 9.1: Rating for the single phase scale-model IGBT-based tap changer.

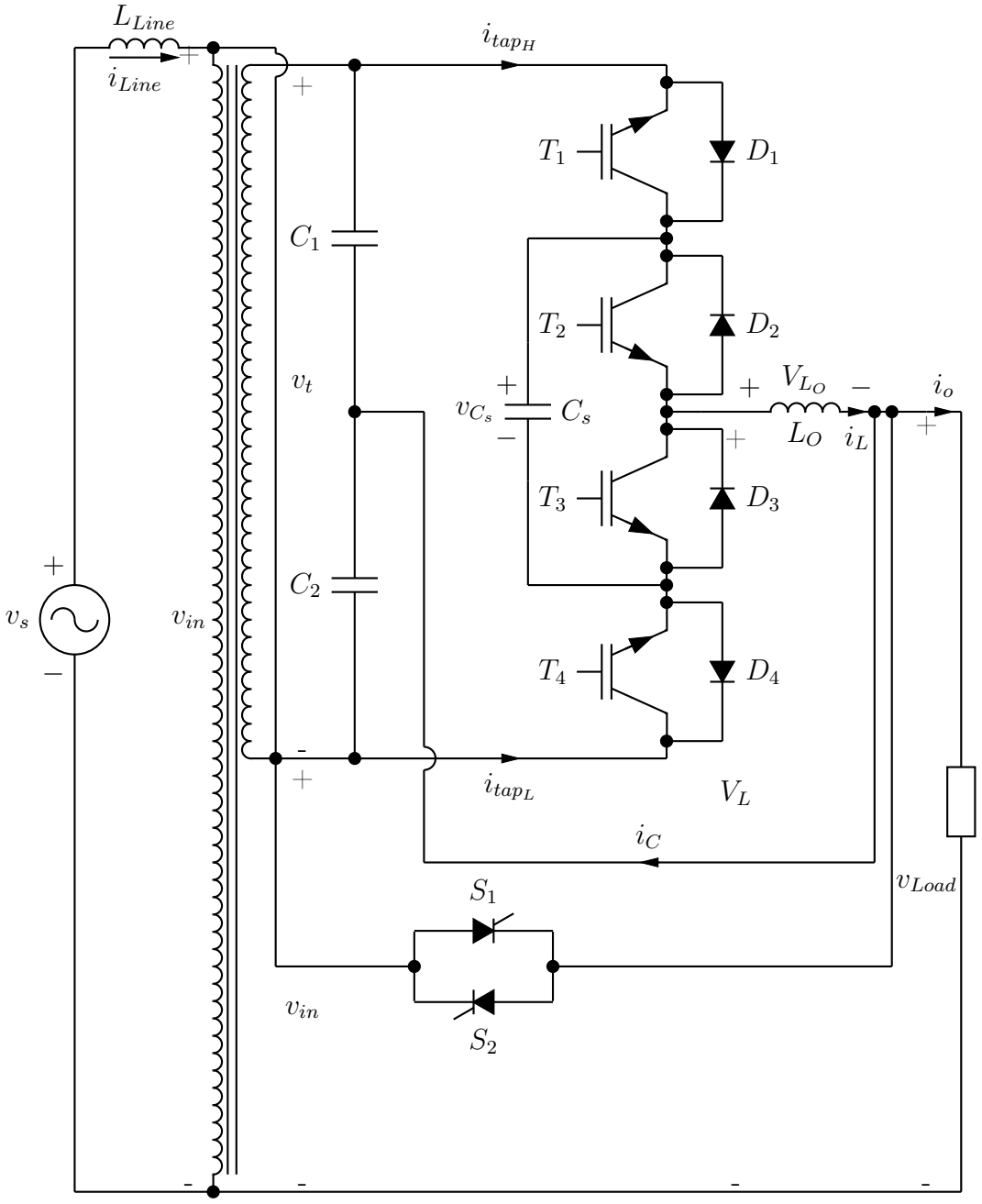

Figure 9.1: Circuit diagram of all the components used for the scale-model IGBT-based tap changer.

Figure 9.2 shows a photo of the full system, indicating the different components of the scale-model IGBT-based tap changer.

Figure 9.3 shows the connection of the IGBT drivers to the IGBTs, which are in turn connected to the sign detector board.

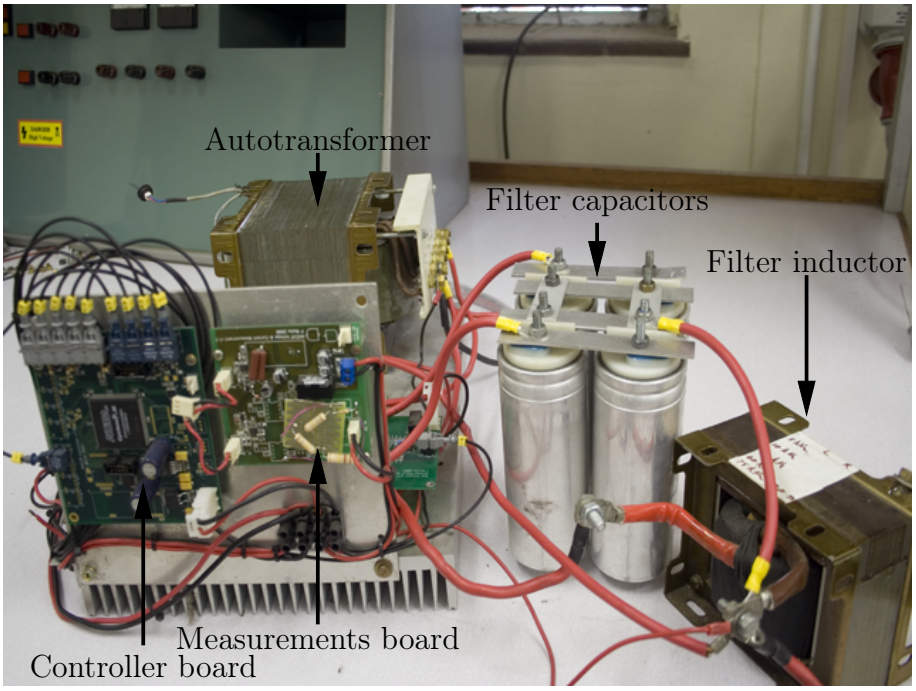

Figure 9.2: Photograph of the scale-model IGBT-based tap changer, indicating the controller board, measurement board, filter capacitors, output inductor, and the autotransformer.

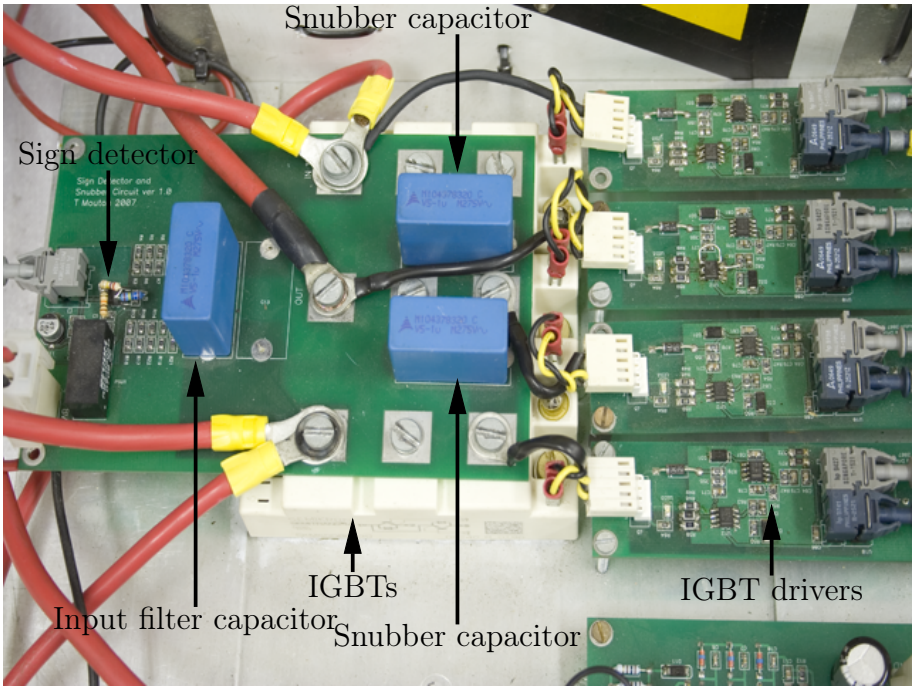

Figure 9.3: Photograph of the connection of the IGBT drivers to the IGBT connected to the sign detector board together with the snubber capacitors.

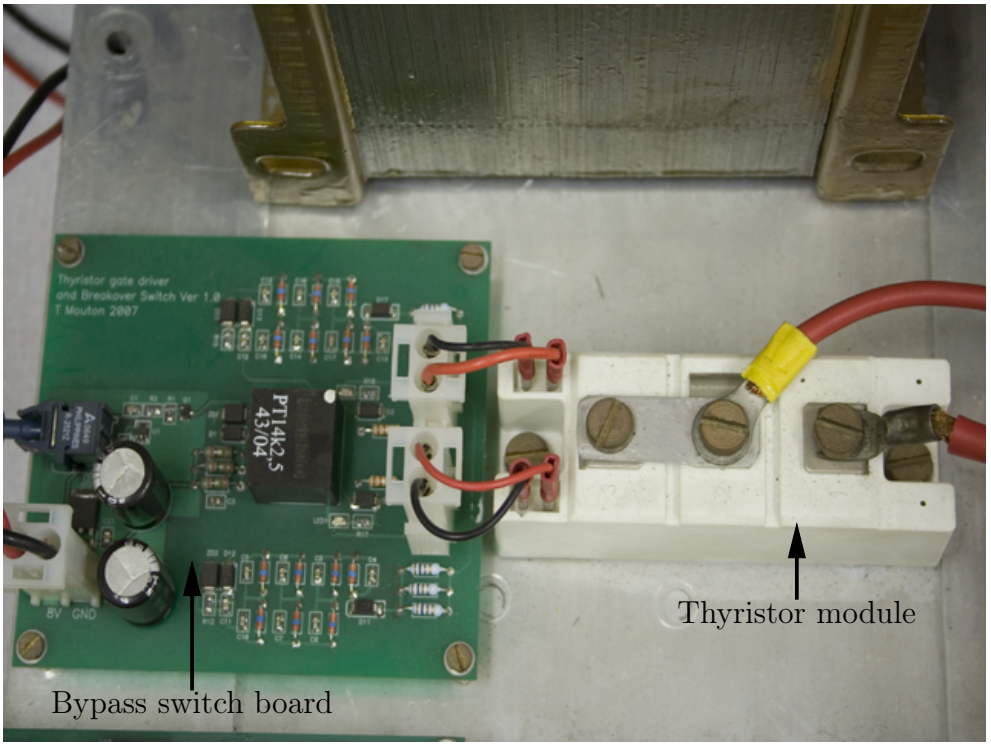

Figure 9.4: Photograph of the connection of the bypass switch together with the thyristor module.

The final photograph in Figure 9.4 shows the bypass switch board connected to the thyristor module.

The autotransformer is equipped with 5 taps rated at 212 V, 222 V, 232 V, 242 V and 252 V. The autotransformer is a single winding autotransformer with the input from the mains connected to the 212 V tap. The scale-model IGBT-based tap changer connects to the autotransformer in a boosting configuration with the scale-model IGBT-based tap changer connected to the 212 V and 252 V taps resulting in a tap voltage of 40 V. The boosting configuration requires a nominal input voltage of 212 V to deliver a 230 V output voltage to the load.

The values of all the passive components together with the model numbers of the different semiconductors are summarised below in Table 9.2.

Description	symbol	Value
IGBT modules	T_1 to T_4 and D_1 to D_4	SEMIKRON SKM50GB063D
Thyristor module	S_1 and S_2	SEMIKRON SKKT 162/12 E
Filter capacitors	C_1 and C_O	50 μF
Output filter inductor	L_O	488.9 μH
Snubber capacitor	C_s	2μF

Table 9.2: Values of the components used in the scale-model IGBT-based tap changer.

9.2 Operational measurements

The measurements conducted and presented in this section cover all the measurable values of the scale-model IGBT-based tap changer with regard to both voltages and currents. These measurements were conducted with the scale-model IGBT-based tap changer operating at a power of 4.8 kW connected to a resistive load, while switching at 10 kHz with a constant 50 % duty cycle. The equipment used for the measurements is shown in Table 9.3.

Description	Manufacturer	Model Number
Oscilloscope	Tektronix	TDS 3014
Voltage probe 1 and 2	Tektronix	TEK P5100 Voltage probe
Current probe 1 and 2	Tektronix	TCP202
Current probe CT	Tektronix	CT4
Power meters 1 and 2	Yokogawa	2533 Digital power meter

Table 9.3: Model numbers and manufacturer of the measurement equipment used.

The process began by measuring the input voltages and currents in and out of the scale-model IGBT-based tap changer, as shown in the image capture from the oscilloscope in Figure 9.5.

The input voltage and current were measured at v_{in} and i_{Line} respectively and are shown in Figure 9.1. The output voltage and current were measured at v_{Load} and i_O, as shown in Figure 9.1. These values were also measured separately with the use of two Yokogawa digital power meters with the results shown below in Table 9.4.

The efficiency of the system is calculated from these measurements using (9.2.1). According to this, the scale-model IGBT-based tap changer has an efficiency of 97.85%.

$$\eta = \frac{Output\ power}{Input\ power} \tag{9.2.1}$$

The measurement depicted in Figure 9.6 focus on the tap voltage and the current flowing through the top and bottom taps, while the scale-model IGBT-based tap changer was operating at the specified power of 4.8 kW.

Figure 9.6 shows the tap voltage and output current provided by the autotransformer to the converter. The tap voltage was measured at position v_t while the high tap current was measured at i_{tap_H} and the low tap current at i_{tap_L}, as indicated in Figure 9.1. It can clearly be seen that the top tap conducts more current than the bottom tap; this is because the top tap being at higher voltage requiring more current to raise the output voltage above the 212 V input voltage. Adding the two tap currents together results in the same output current showing that the output current is split between the two taps.

The effect of the switching is clearly visible in Figure 9.6: all the waveforms show a top and bottom envelope as the IGBTs switch between the top and bottom taps.

The next measurement, illustrated in Figure 9.7, looks at the voltage over the snubber capacitor, as well as the inductor current and the output current.

The measurement shows the influence that the switching scheme has on the operation of the snubber capacitor. During the positive half-cycle, when IGBTs T_1 and T_4 are switched on permanently, the snubber capacitor is connected in parallel with the filter capacitors, thus allowing the snubber capacitor to filter the tap voltage. During the negative half-cycle, when IGBTs T_2 and

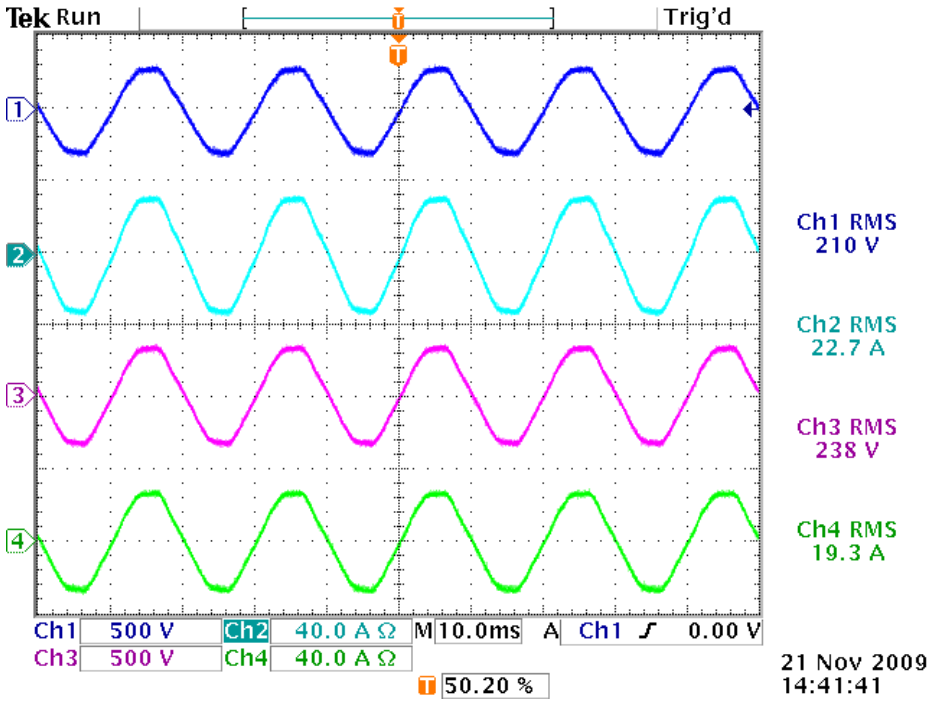

Figure 9.5: Measurement of the input voltage (Dark Blue) and current (Light Blue) together with the output voltage (Purple) and current (Green).

Description	Value
Input voltage	212.3 V
Input current	22.667 A
Input active power	4.790 kW
Output voltage	238.6 V
Output current	19.660 A
Output active power	4.687 kW

Table 9.4: Input and output measurements made with the power meters

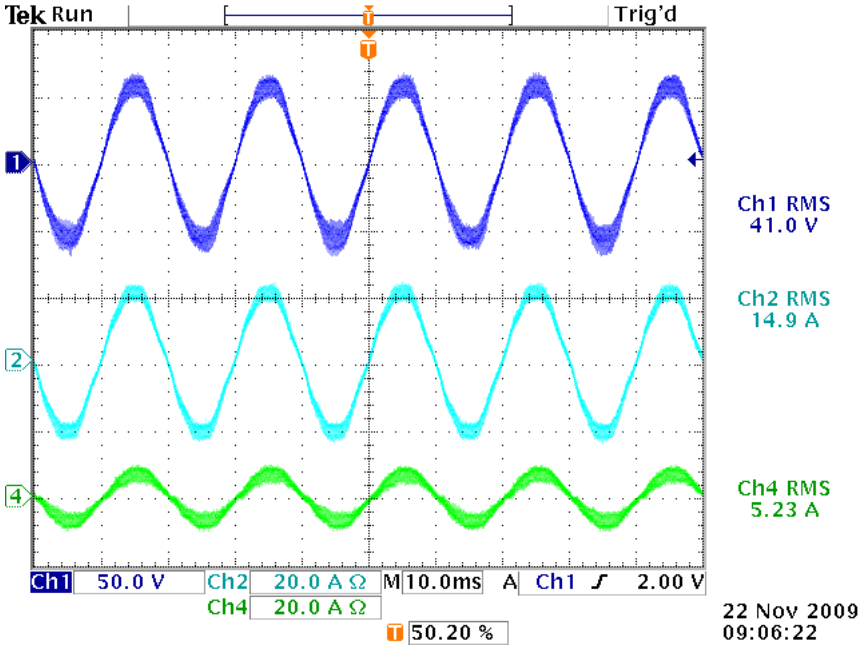

Figure 9.6: Measurement of the tap voltage v_t (Dark Blue) and the tap currents for the high tap position i_{tap_H} (Light Blue) and low tap position i_{tap_L} (Green).

T_3 are switched on permanently, the capacitor is short-circuited and unable to perform filtering. Both of these behaviours are clearly visible from the waveform of the snubber capacitor voltage shown in Figure 9.7.

The measurement result also shows the inductor current together with the output current. These currents are measured at the same time to show that the inductor has a ripple component that is not present in the output current. The switching of the IGBTs between the two taps can clearly be seen in the inductor current, as the current shows both top and bottom switching envelopes. The measurement shown in Figure 9.8 shows only the inductor current, with the switching clearly visible at the peaks of the inductor current, which is as expected.

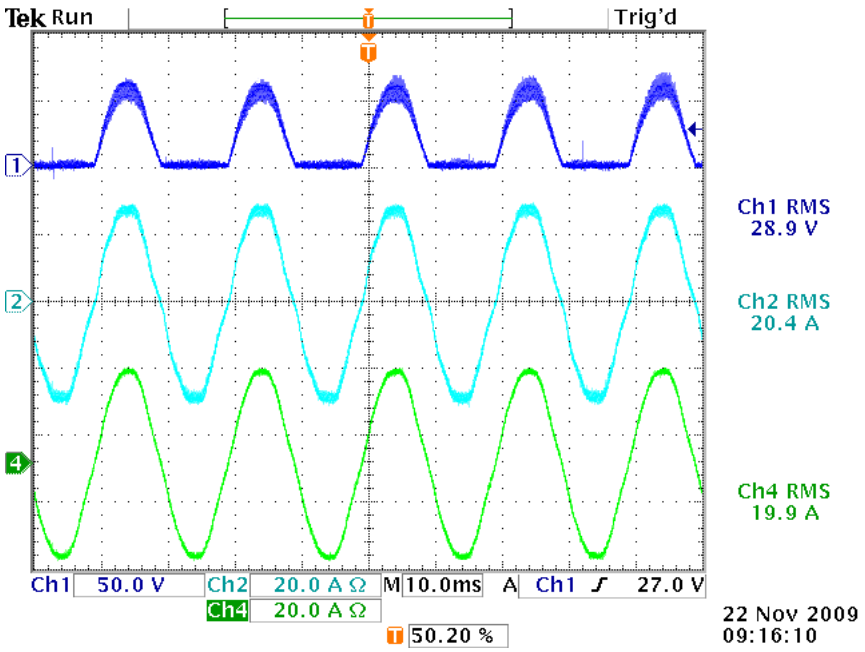

Figure 9.7: Measurements of the snubber capacitor voltage v_{C_s} (Dark blue), inductor current i_L (Light Blue) and the output current i_O (Green).

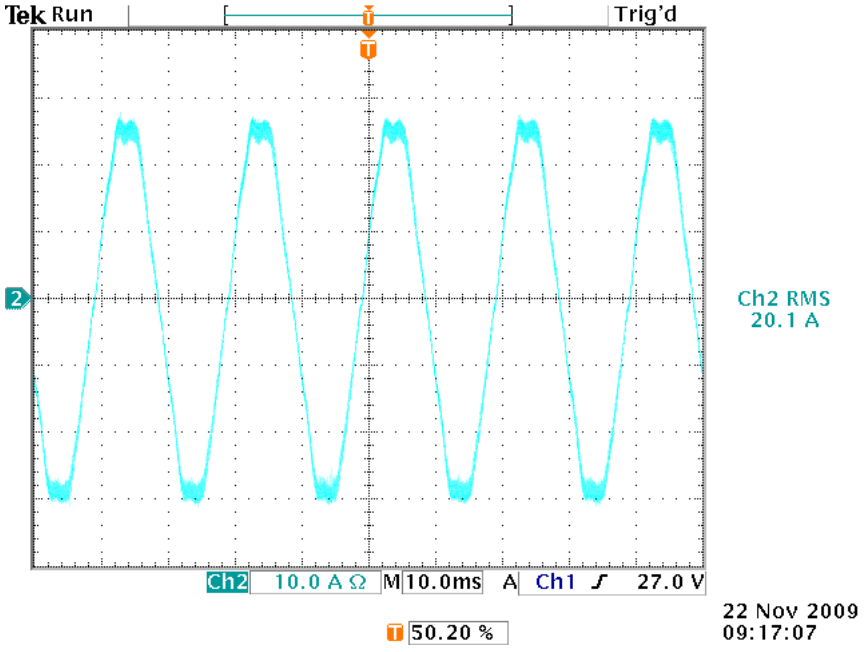

Figure 9.8: Inductor measurement showing the inductor ripple current at the peaks of the waveform.

The fact that the output current does not show a ripple component, verifies that the filtering done through the connection of capacitors C_1 and C_2 together with inductor L_O is sufficient. The measurement conducted on the snubber capacitor voltage verified that the switching scheme works as proposed.

The next section looks at the control of the output voltage by designing a new compensator specifically for the scale-model IGBT-based tap changer.

9.3 Control measurements

In order to verify that the controller designed in Chapter 7 works in the scale-model IGBT-based tap changer, the controller had to be redesigned with respect to the different passive components used in the scale-model IGBT-based tap changer. However, designing the compensator requires the series winding leakage inductance of the 5 kVA autotransformer to be calculated first. The method described in Section 5.1.1 of Chapter 5 was therefore used to calculate the leakage inductance of the series winding by means of conducting the short-circuit test on the series winding.

The results from the measurements are provided in Table 9.5 below.

Description	**Value**
Input voltage	1.3 V
Input current	19.2 A
Input active power	18 W
Output current	16.1 A

Table 9.5: Results from the short circuit tests using both the power meters for the measurements

Accoring to (5.1.5)[1], the autotransformer draws 17.292 VAR of reactive power. Using (5.1.7) and (5.1.8)[2] determines the total winding resistance at 0.049 Ω and the total winding leakage reactance at 0.047 Ω. In order to separate the series winding reactance from the common winding reactance, the current factor in (5.1.9)[3] must have a value of 0.839. The resulting leakage reactance of the series winding is calculated with (5.1.13)[4] with a value of 0.007 573 Ω. Finally, the series winding inductance is calculated with (5.1.14)[5] results in a value of 24.107 μH. The resulting resistance of the series winding is calculated with (5.1.11)[6] to be 0.008 Ω.

[1]See page (5.1.6)
[2]See page 66
[3]See page 67
[4]See page 68
[5]See page 68
[6]See page 67

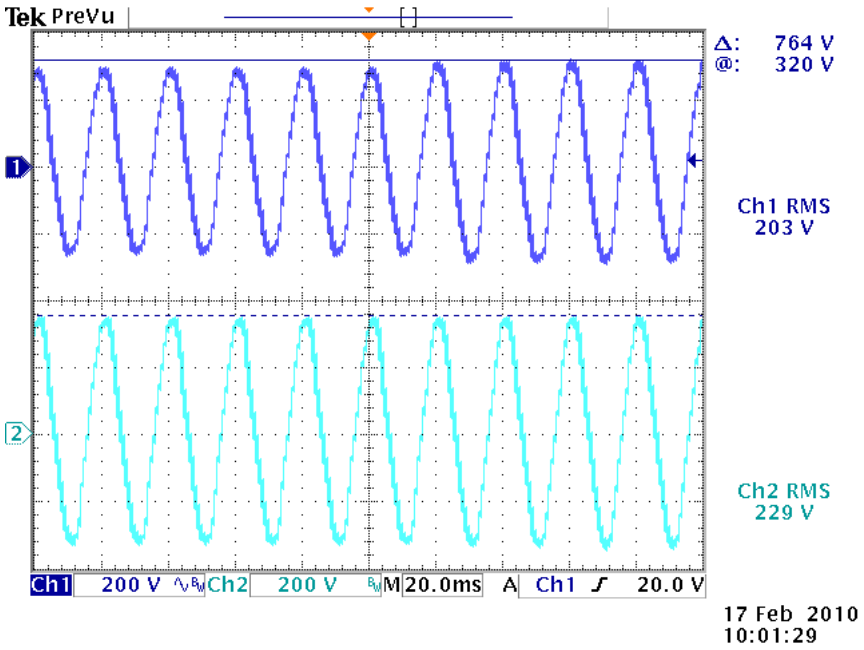

Figure 9.9: Regulated output voltage (Light Blue) while correcting the waveform while applying a instantaneous 20 V step to the input voltage (Dark blue).

The same design methodology as that present in Chapter 7, namely, the *design by emulation* [29] technique, is used to design and implement the feedback controller for the scale-model IGBT-based tap changer into the same FPGA. The design of the compensator for the scale-model IGBT-based tap changer is shown in Appendix A.

The final compensator is shown in (9.3.1) below:

$$\begin{aligned} d(k) &= \frac{5.000\ 47}{v_t}\Big(error(k) - 1.941 error(k-1) + 0.985\ 7 error(k-2)\Big) \\ &\quad +1.169 d(k-1) - 0.168\ 8 d(k-2) \end{aligned} \tag{9.3.1}$$

Testing the compensator on the scale-model IGBT-based tap changer resulted in poor performance, with the scale-model IGBT-based tap changer performing no regulation.

After multiplying the gain of the compensator with 25, however, the scale-model IGBT-based tap changer did successfully regulate the load voltage, while improving the waveform. Figure 9.9 shows the measurements conducted on the scale-model IGBT-based tap changer with the compensator added.

This measurement shows that the designed compensator is able to control the scale-model IGBT-based tap changer to such an extent that the output voltage can be regulated while correcting the output waveform. The controller is also capable of regulating the output voltage within a single cycle of the input voltage when a step change is applied.

9.4 Summary

This chapter looked at the practical measurements that were used to validate and verify the concept of the IGBT-based tap changer by means of a scale-model. Practical measurements were done on the input and output voltage and currents, as well as assessing the efficiency of the scale-model IGBT-based tap changer. The chapter also measured the currents provided by the taps of the autotransformer to the converter. The resulting waveform shown for the voltage over the IGBTs proves that the converter in the scale-model IGBT-based tap changer does work successfully. The measurement of the snubber capacitor voltage shows the effect of the switching scheme on the capacitor. The final measurements tested the performance of the compensator that had been designed specifically for the calculated leakage inductance of the selected autotransformer.

Chapter 10

FPGA embedded software design

In order to ensure that the IGBT-based tap changer switches at the correct frequency and in order to regulate the output voltage, the FPGA had to be programmed with the appropriate embedded software. This software controls the IGBTs that are used inside the IGBT-based tap changer by means of a specifically designed set of processes. Utilising the different fault and sign signals and the output voltage measurements, these processes are able to control the IGBT-based tap changer.

This chapter looks at the software features that were implemented on the FPGA to control the IGBT-based tap changer. As a useful starting point, this chapter gives an overview of all the different components used on the FPGA. Thereafter, the different processes that are used to control the IGBT-based tap changer are reviewed. The list below briefly mentions each of the processes used.

- PWM generation process: This process generates the PWM for the top and bottom IGBTs.
- Commutation process: Controlling the gating signals of all four of the IGBTs makes this the most important and vital process on the FPGA.
- Protection process: Protection of the IGBTs is particularly important for the IGBT-based tap changer. This process monitors the fault signals received from the IGBT driver circuit boards, and it responsible for disabling the PWM if a fault occurs.
- ADC process: Generating the clock and chip select signals for the ADC allows this process to select which channel the ADC must convert. This converted value is then used by the control process.
- Control process: Controlling the output voltage of the IGBT-based tap changer is critical for providing a regulated output voltage. Using the

ADC measurement together with the control algorithm derived in Chapter 7 to set the duty cycle of the PWM furthermore regulates the output voltage of the IGBT-based tap changer.

10.1 The Altera EP3C25Q240C8 FPGA

The FPGA implemented to control the IGBT-based tap changer is an Altera manufactured FPGA. Table 10.1 summarises the relevant specifications of this FPGA.

Description	Value
Logic elements	24 624
M9K embedded memory blocks	66
Total RAM (Kbits)	594
Embedded 18-bitx18-bit multipliers	66
Phase-lock-loops (PLL's)	4
Pin count	240
Maximum user I/O pins	148

Table 10.1: Altera EP3C25Q240C8 [6] FPGA Specifications.

The programming language used to program the embedded software for the FPGA is VHDL. Programming in VHDL is done within the Quartus II V9.2 software development environment made available by Altera; this is designed specifically for Altera FPGAs.

Quartus II compiles the VHDL code and optimizes it for the specific FPGA selected. It also checks that the design timings as well as the indicated clock input will work for the specific FPGA. The programming files generated by Quartus II are uploaded to the FPGA via the JTAG interface through an Altera USB-blaster programmer. The FPGA begins to operate immediately after is has been programmed. Storing the program code on the EPCS16 configuration device allows the FPGA to start operating directly after the controller board has powered up.

Loading the program code onto the EPCS16 device is accomplished by means of two different methods. The first method loads the program code directly onto the EPCS16 device through an Active serial port, whereas the second method loads the program code through the FPGA connected to the JTAG interface. This second method simplifies the controller board layout because it does not require the Active serial programming port to be installed.

Programming the FPGA in VHDL allows multiple processes to be created, all of which can operate in parallel to each other. Running from the same clock source synchronizes the processes with each other, allowing control signals to

flow between the different processes. These control signals allow one process to start after another has finished.

Control signals do not originate from within the FPGA only. Fault signals and other control signals sent by different components are also able to enter the FPGA. However, these signals are not synchronized with the clocks of the different processes, and may potentially false trigger the processes to which they are connected, which will negatively influence the operation of the FPGA. It is thus vital to synchronize the external input signals to the FPGA by clocking them through a flip-flop. The flip-flop clocks these signals into the FPGA on the rising edge of the system clock, synchronizing the input signals with the rest of the FPGA. This allows the input signals to change without affecting the operation of the FPGA.

Using different clock sources for different processes requires these clock sources to be synchronized as well. Clock skew occurs when they are not synchronized, which will lead to processes executing in an unsynchronized fashion. Synchronizing the clocks in the FPGA is done by means of a phase-lock-loop (PLL) together with a clock domain setup in Quartus II. The clock domain setup in Quartus II informs the timing analyser which clock must be compensated for while performing the timing analysis for the specific FPGA. The input clock into the FPGA is used as the clock domain for the timing analyser before it enters the PLL. Using a 24.576 MHz crystal oscillator for the input clock for the FPGA and PLL allows the derived clocks to be generated by a single PLL, as shown in Table 10.2.

Clock name	**Multiplier**	**Resulting clock (MHz)**
System clock	x 1	24.576
PWM clock	x 2	49.152
ADC clock	÷ 5	4.915

Table 10.2: PLL output clocks.

Running the system clock through a so-called 'times one multiplier' in the PLL allows the system clock to be synchronized with the other clock outputs of the PLL. Using the PWM clock at a frequency of 49.152 MHz furthermore allows the PWM to be generated at double the resolution than for the 24.576 MHz clock. The ADC operates with a 4.915 MHz clock, which is well below the 20 MHz limit [31] of the ADC. A 4.915 MHz clock allows the ADC to provide over three hundred thousand samples per second, which is adequate for the IGBT-based tap changer.

Setting up Qaurtus II to synchronize the clocks through the PLL together with the single clock domain is vital, as is clocking the input signals into the FPGA. Using these settings as well as the parallel processes allows the FPGA to control the IGBT-based tap changer by means of the processes below. The

following sections describe the processes that are used to control the IGBT-based tap changer, using flow charts to illustrate the flow of each process.

10.2 PWM generation process

The generation of the PWM signals for the IGBT-based tap changer is vital for the correct operation of the tap changer. This process generates the PWM while also including the dead time. The 49.152 MHz PWM clock generated by the PLL is used to drive a counter that counts from 0 to 4916, thus generating a 10 kHz signal. Figure 10.1 shows the diagram used to determine the switch-on and -off positions for the top and bottom PWM signals (referred to as PWM TOP and PWM BOTTOM).

Each cycle of the PWM starts with the PWM counter value at 0. The PWM is in a dead time zone between 0 and 123 of the PWM counter, resulting in 2.5 μs dead time. With the duty cycle set at 50%, the PWM TOP signal can be switched on until the PWM counter reaches the PWM cycle 1 value. The PWM cycle 1 value is switched off for the PWM TOP signal and is determined, by the following equation:

$$\text{PWM cycle 1} = \text{Duty cycle} * 4\,916 - 123 \tag{10.2.1}$$

PWM TOP switches off at the PWM cycle 1 position and enters the dead time period between the PWM TOP and PWM BOTTOM signals. The PWM BOTTOM signal switches on after the PWM counter has counted 246 cycles on from the PWM cycle 1 at position PWM cycle 2. Equation 10.2.2 below shows the equation used to derive the position for PWM cycle 2.

$$\text{PWM cycle 2} = \text{Duty cycle} * 4916 + 123 \tag{10.2.2}$$

PWM BOTTOM switches on at PWM cycle 2 and switches off before the dead time for the next switching cycle starts. Starting the dead time at

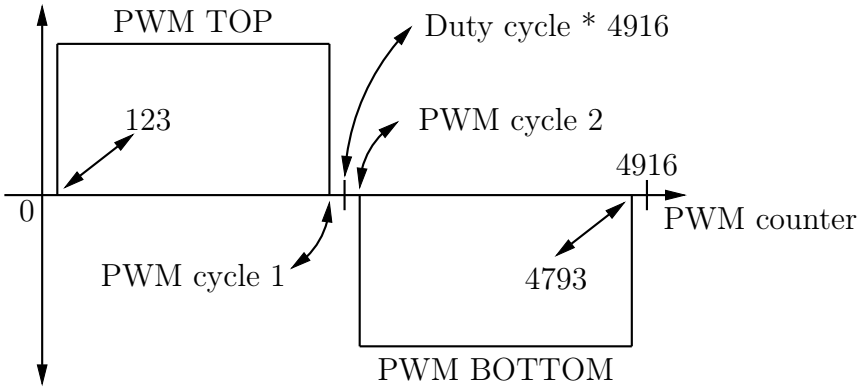

Figure 10.1: PWM generation diagram

123 cycles of the PWM counter before the end of the cycle forces the PWM BOTTOM signal to switch off at 4793 cycles of the PWM counter. The final dead time section lasts only 2.5 μs as the PWM counter counts 123 cycles from 4793 to 4916 where the PWM counter is set back to 0 and the switching cycle starts over again.

The implementation of dead time influences the effective percentage of duty cycle that can be applied. If the duty cycle is set below 5.004%, then the PWM TOP signal will not switch on for the entire switching cycle. This happens becuase the PWM cycle 1 is positioned before the 123 dead time count value. The same occurs for a duty cycle higher than 94.996%, which results in the PWM BOTTOM signal never switching on, with the PWM cycle 2 positioned after the 4793 position.

With the duty cycle effectively operating between 5.004% and 94.996%, PWM BOTTOM signal remains turned on permanently without any dead time for duty cycles below 5.004%. Duty cycles above 94.996% will result in the PWM TOP signal being switched on permanently. This is implemented in the commutation process and not in PWM generation process.

The PWM is generated through a single process that runs from the PWM clock at 49.152 MHz. Figure 10.2 shows the flow diagram of the process used to generate the PWM signals. The process starts by incrementing the PWM counter with one each time the process repeats it self. Going through the conditions as shown in Figure 10.2 allows the process to determine which PWM signal must be switched on or off. The list below contains the statements used for each of the conditions in the flow chart.

- Condition A: PWM counter $>$ 0 and PWM counter $<$ 123
- Condition B: PWM counter $>=$ 123 AND PWM counter $<$ PWM cycle 1
- Condition C: PWM counter $>=$ PWM cycle 1 and PWM counter $<$ PWM cycle 2
- Condition D: PWM counter $>=$ PWM cycle 2 and PWM counter $<$ 4793
- Condition E: PWM counter $>=$ 4793 and PWM counter $<$ 4916
- Condition F: PWM counter $>=$ 4916

10.3 Commutation process

Switching the IGBTs in the correct order at the correct times is vital to the correct operation of the IGBT-based tap changer. This process controls the

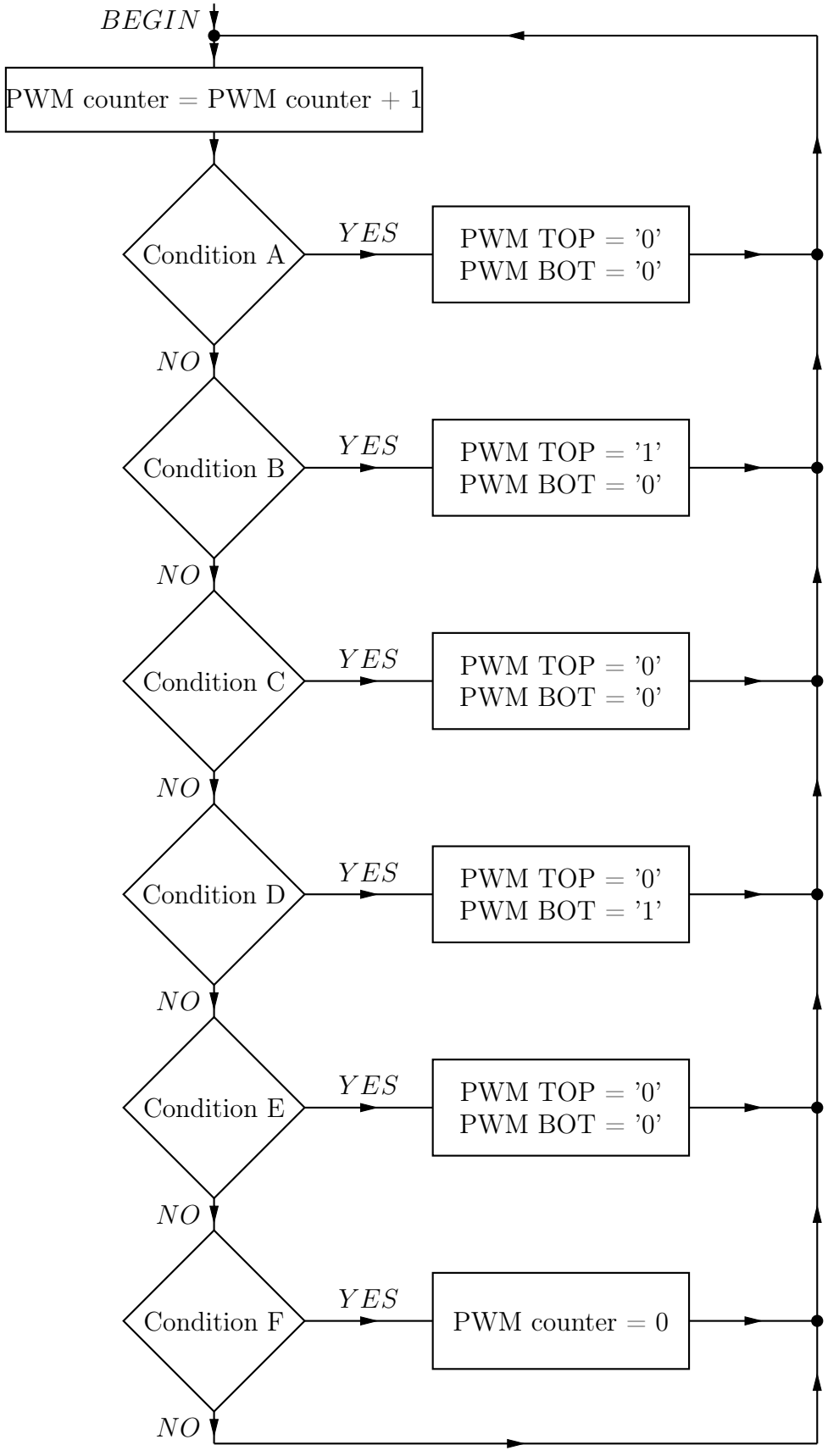

Figure 10.2: Flow chart of the PWM generation process.

switching of the IGBT pairs by means of the signal provided by the sign detector circuit board with regard to the switching pattern presented in Chapter 2.

Controlling the IGBTs by means of the switching pattern presents one important problem though. Changing between the two switching pairs of the IGBTs during the zero voltage crossover of the input voltage can potentially short-circuit the autotransformer. Switching over between the two IGBT pairs at the same instant does not leave enough time for the one pair of IGBTs to switch off before the other switches on. The IGBT pair that is busy switching off takes a considerable amount of time to switch off properly while the other IGBTs is already switching on, which results in the autotransformer being short-circuited. The dead time must be incorporated into the commutation process during the zero voltage crossover of the input voltage.

The commutation process also controls the waveform generator executed in the FPGA, by generating a 50 Hz sinusoid that is used by the feedback control. The waveform generator needs to reset every time the input voltage changes from negative to the positive polarity in order to synchronize the generator with the input voltage. The waveform generator reset signal 0 resets the waveform generator.

Running the commutation process through an external counter makes it relatively easy to control the flow through the process. The counter also helps with the implementation of the dead time as well as protecting against any glitches received from the sign detector circuit.

Figure 10.3 shows the flow chart for the commutation process while the list below describes the statements for the conditions.

- Condition A: Sign counter $>$ 235 000 AND sign previous != sign
- Condition B: Sign counter $>$ 0 AND Sign counter $<$ 246
- Condition C: Sign counter $>$ 246

The process starts by checking for a change in the signal received from the sign detector. If the counter for the commutation process has passed 235 000 and the sign signal changes, it resets the counter, switches off all IGBTs and resets the waveform generator.

The process thereafter advances to condition B if the signal from the sign detector has not changed state. Continuously entering condition B while the sign counter is between 0 and 246 implements dead time for a period of 5 μs.

Entering condition C for the sign counter values above 246 permits the IGBT-based tap changer to operate as required. Checking the value of the signal received from the sign detector together with the duty cycle determines which IGBTs are switched on or off.

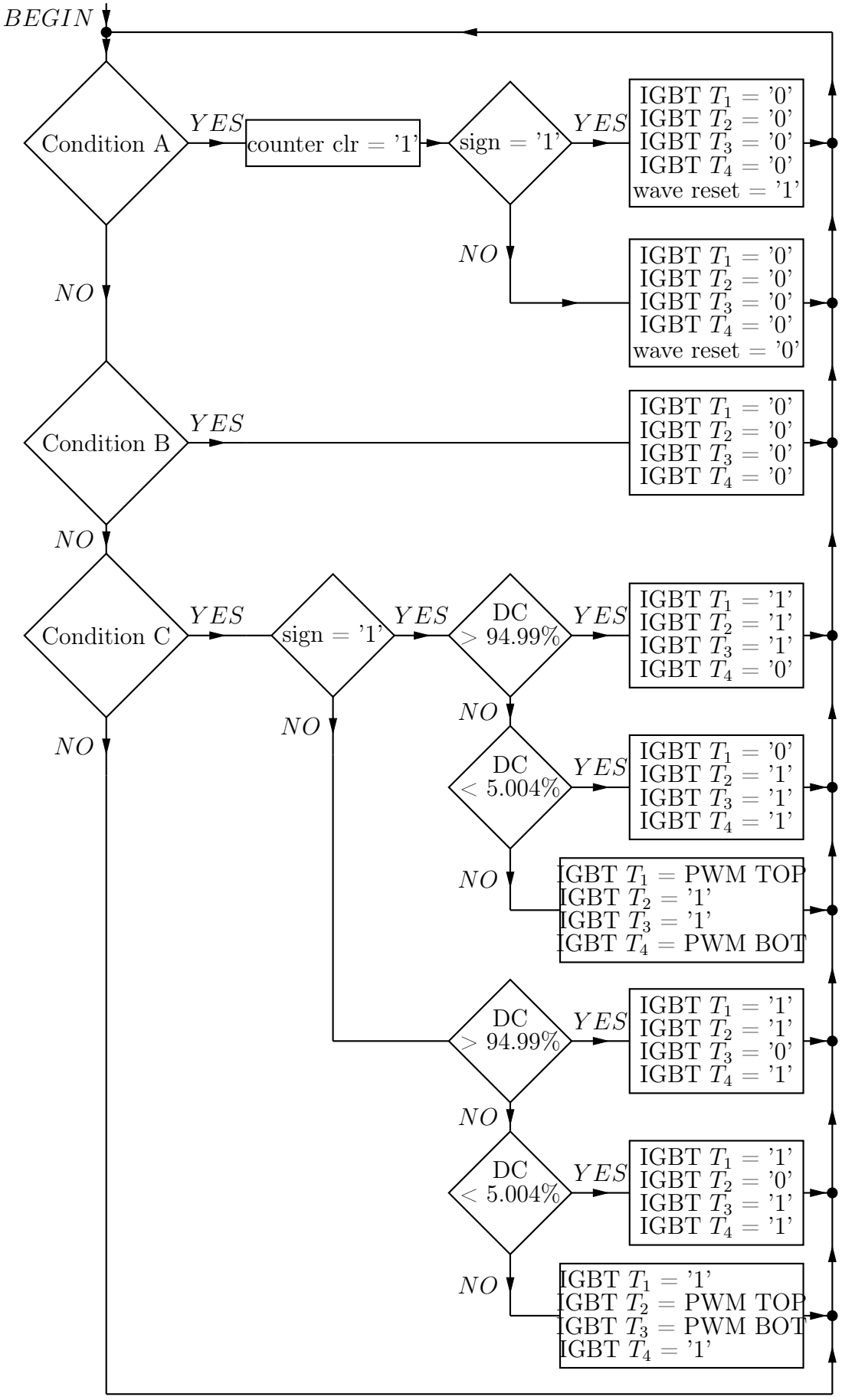

Figure 10.3: Flow chart of the commutation process.

10.4 Protection process

Protecting the IGBTs in the IGBT-based tap changer against damage is critical. Protection against over-currents is done through the FPGA by either measuring the output current of the IGBT-based tap changer or by tracking and responding to fault signals received from the IGBT driver boards.

The IGBT drivers detect whether the current conducted by the IGBT is greater than the rated current of the IGBT by measuring the on-state voltage V_{ce} of the IGBT. If the voltage exceeds this maximum, the IGBT driver sends a fault signal to the FPGA. The FPGA receives the signal and starts to transfer the current from the IGBTs to the thyristors.

The flow chart in Figure 10.4 shows the flow of the protection that transfers the current between the IGBTs and the thyristors. The list below provides the statements for each of the conditions in the flow chart.

- Condition A: IGBT 1 Fault = 1 OR IGBT 2 Fault = 1 OR IGBT 3 Fault = 1 OR IGBT 4 Fault = 1 OR Output current > max output current
- Condition B: IGBT 1 Fault = 0 AND IGBT 2 Fault = 0 AND IGBT 3 Fault = 0 AND IGBT Fault = 0 AND Output current < max output current
- Condition C: -1 < output current < 1

As the protection process it monitoring both the fault signals of the IGBT drivers and the output current of the IGBT-based tap changer, it is able to switch off the IGBTs and switch on the thyristors at any moment. If a fault signal appears the PWM signals will be turned off and thyristors will be switched on, after the switch-off dead time period for the IGBTs has passed.

Entering condition B after the output current has dropped below the rated limit of the IGBTs and after the fault signals have been cleared, switches off the gating signal to the thyristors. The thyristor only stop conducting and switches off after the current flowing through it has reached 0 with the gating signal removed. The protection process thus waits until the load current has reached 0 before it switches the PWM signals back on.

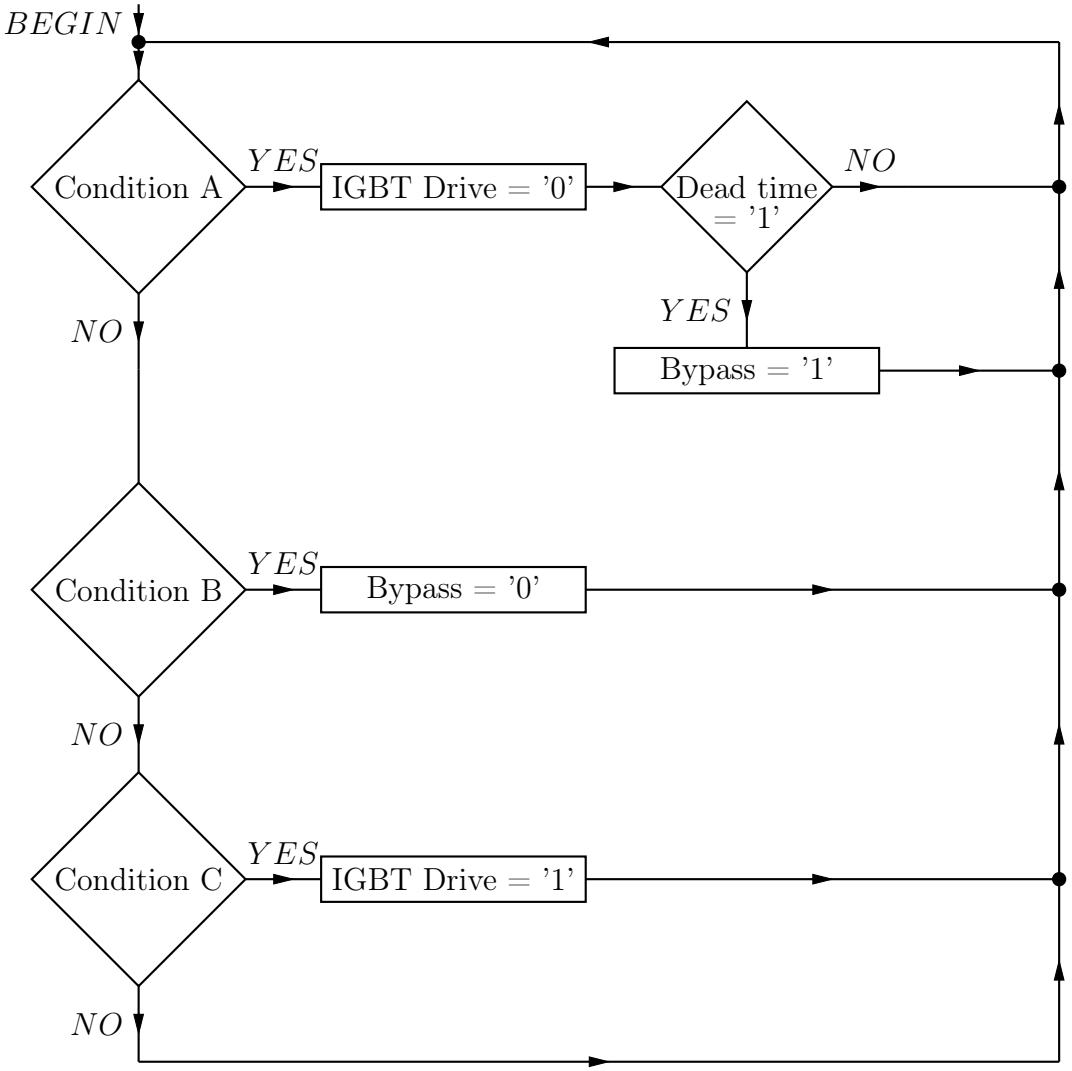

Figure 10.4: Flow chart of the protection scheme.

10.5 ADC process

The ADC process generates the signals required by the AD7924 ADC on the controller board. This ADC measures the output voltage and current required by the FPGA to control and protect the IGBT-based tap changer.

The AD7924 [31] runs from the 4.915 MHz clock generated by the PLL of the FPGA. It also requires a chip select signal in order to operate and perform conversions. Connecting the chip select signal to ground informs the ADC that it must send out the value of the converted channel and that it must prepare to receive a new command. Connecting the chip select signal to +3.3 V allows the ADC to perform a conversion of the selected channel.

The operation of the ADC process is based on a state machine running on the 24.576 MHz system clock. The ADC process also controls two shift

registers; one of these receives a 12-bit variable to control the ADC and outputs this value via a serial data stream synchronised to the 4.915 MHz clock. The other shift register clocks in the data received from the ADC and outputs data in 15-bit format. The data stream contains the channel measured by the ADC, as well as the conversion value of the specific channel.

Generating only the required control signals to control the ADC simplifies the implementation of the ADC process. Figure 10.5 shows the relevant flow chart.

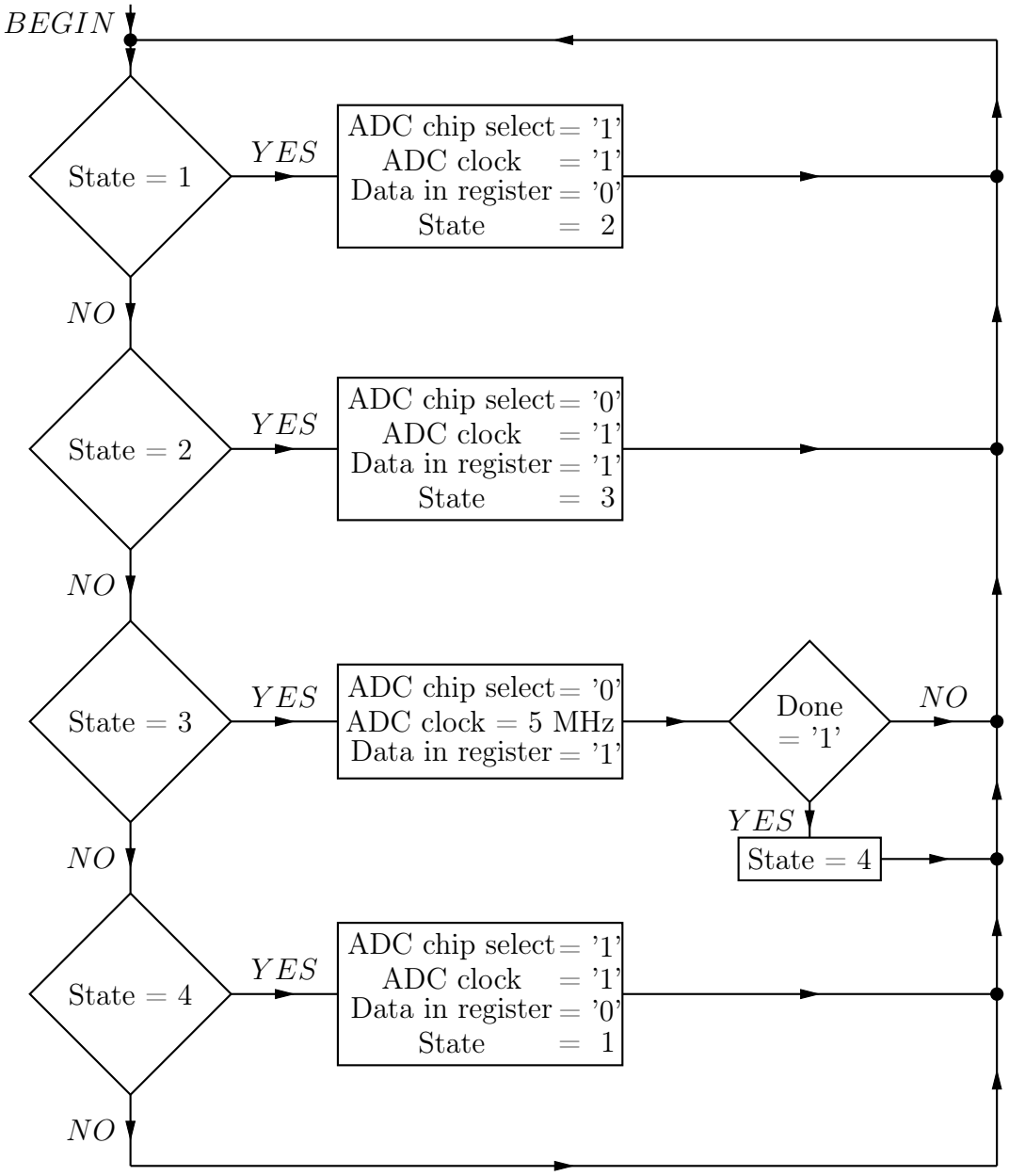

Figure 10.5: Flow chart of the ADC process.

At State 1, the ADC performs a conversion on a channel due to the chip select signal, which is driven by a logic high while driving the clock high too. Driving the clock with a constant logic high does not influence the ADC because the chip select signal which also driven high; the ADC only requires the clock signal when the chip select is driven with a logic low. Driving the 'register enable' signal with a logic low disables the shift registers from shifting any data either in or out.

Entering State 2 after one clock cycle of the system clock drives the chip select signal for the ADC with a logic low, while activating the shift registers. Continuing to drive the ADC clock signal with a logic high conforms to the clocking requirements [31] of the ADC to operate correctly.

State 3 drives the ADC clock signal with the 4.915 MHz clock with the chip select low and the shift registers enabled. These allow the ADC to receive data from one shift register while transmitting data to the other shift register at the same moment. All the registers run on the same 4.915 MHz clock used for the ADC, which thus synchronises all these components.

Running the ADC process on a different clock than the ADC itself presents another problem with regard to knowing when 16 cycles of the 4.915 MHz clock have elapsed. A separate process is therefore created to count the clock cycles of the 4.915 MHz clock until it reaches 16 and to inform the ADC process by means of a 'Done' signal.

Exiting State 3 after receiving the 'Done' signal from the clock counting process allows the ADC process to enter state 4. This allows the ADC to perform the next conversion with the chip select signal driver with a logic high. The ADC process also disables both the shift registers by driving the *register enable* signal with a logic low.

The ADC process returns to State 1 after State 4 has ended, restarting the entire conversion process.

10.6 Feedback control process

The feedback control process implements all the final elements and equations that are necessary to control the IGBT-based tap changer. It receives measurement data from ADC and reference data from the waveform generator and scales these values for easier insertion into the equations. These equations are then used to determine the duty cycle for the next switching cycle of the IGBT-based tap changer. Using all of these elements together gives the IGBT-based tap changer the ability to regulate the output voltage provided to the load.

This process operates from the 4.915 MHz clock in order to leave enough time for the equations to perform their calculations and store the results. Running this process from the 24.576 MHz clock, however, delivers incorrect mathematical results, causing poor regulation of the system.

Using a state machine to control the flow through the process simplifies the implementation of the process in VHDL. Figure 10.6 shows the flow chart for the control process.

The process starts with State 1 scaling both the ADC measurement and the waveform generator outputs into values of the same magnitude. The scaled down output voltage of the IGBT-based tap changer, which is between 0 and 2.5V is then measured by the ADC. This voltage is read as a 12-bit two's complement value, which has a maximum value of 2047 multiplied with 0.198 to deliver a 325 V peak measurement. Multiplying the 12-bit two's complement output of the waveform generator with 0.158 delivers a 325 V representation of the reference voltage. Multiplying the same waveform generator output with 0.027 delivers a 40 V representation of the tap voltage.

Scaling these values to the same range make is easier to execute the mathematics for the control process. Splitting the calculations of the mathematics furthermore allows the FPGA to calculate the duty cycle for the next switching cycle in phases.

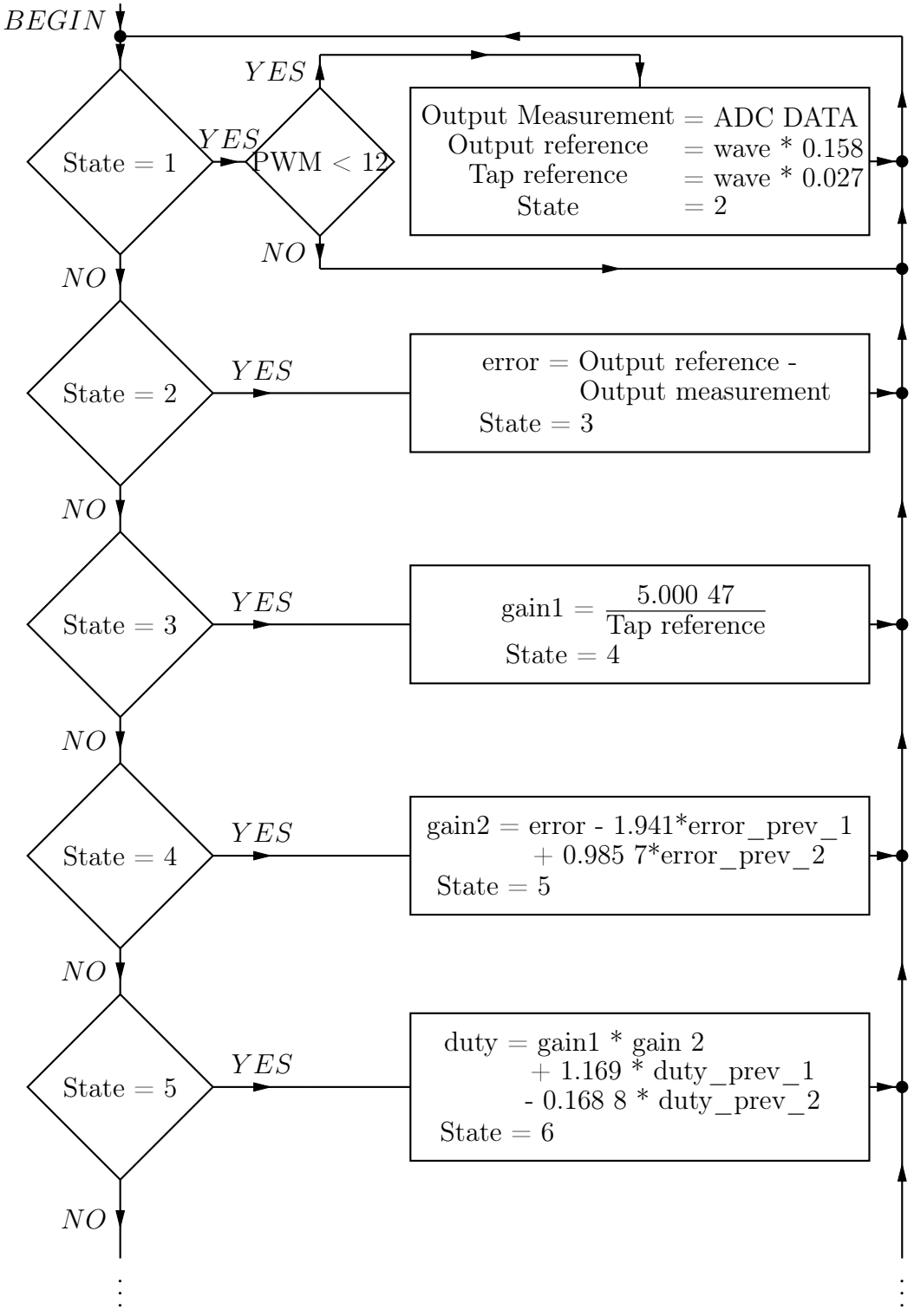

Figure 10.6: Flow chart of the control procedure.

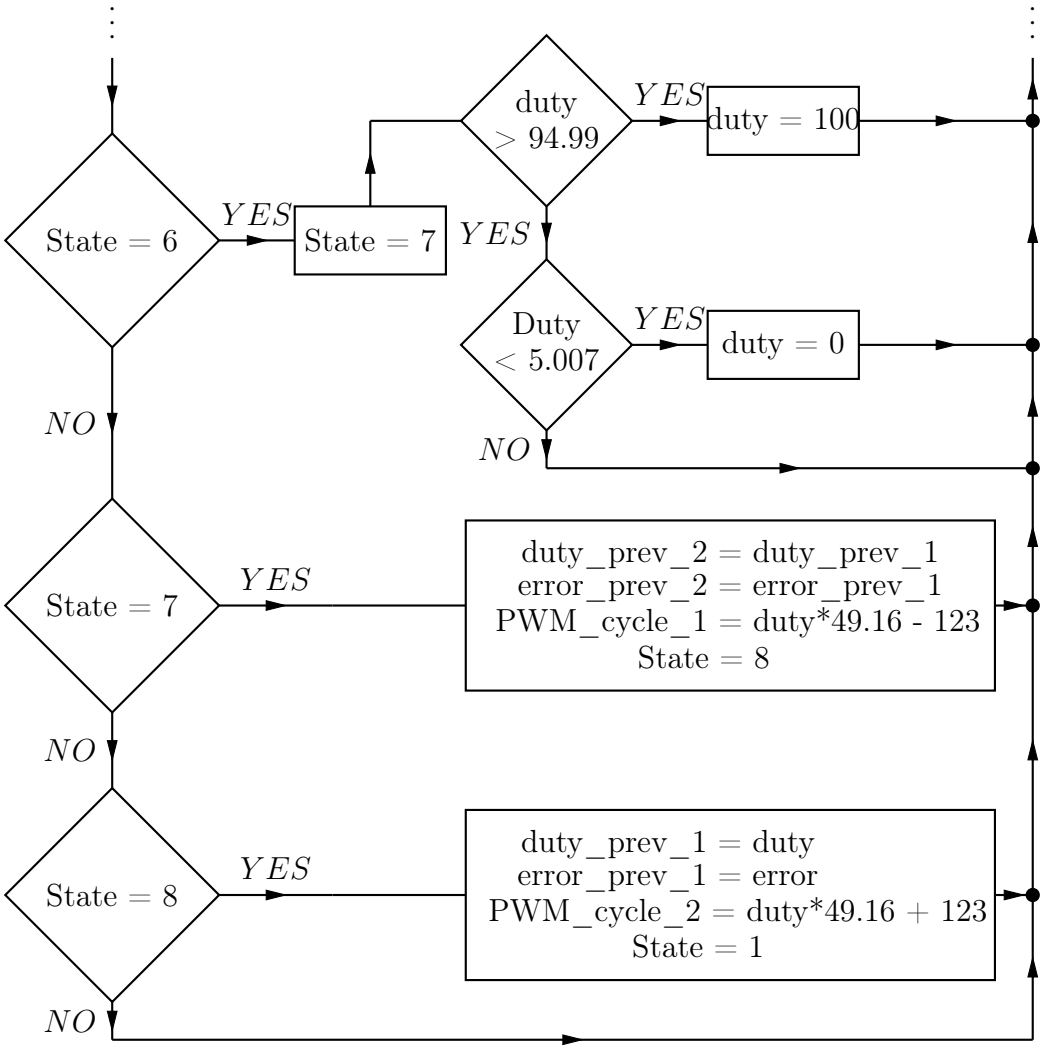

Figure 10.7: Continued flow chart of the control procedure.

This process also implements integrator anti-windup. Using the anti-windup prevents the integrator from running away from the required values. It is done by clamping the maximum and minimum duty cycle values to either 0 % or 100 %. This prevents the duty cycle set by the controller from disrupting the control algorithms.

10.7 Summary

This chapter has looked at the software that was implemented on the FPGA to control the switching of the IGBTs in the IGBT-based tap changer. The chapter looked at the most important processes used inside the FPGA and began by focusing on the process used to generate the PWM signals. This was

followed by an examination of the commutation process, which was followed by a discussion of the protection process. Thereafter, the ADC process was analysed, and lastly, the chapter ended by presenting the control process.

Chapter 11

Conclusions

This chapter gives a brief overview of the IGBT-based tap changer designed in this thesis. The design of the hardware as well as the software is covered. The chapter concludes by discussing the results gathered from simulation and the testing conducted on the scale-model IGBT-based tap changer.

11.1 Overview

The design of a solid-state tap changer for MV networks presents with a couple of challenges: namely, the high voltages and currents of MV networks makes component selection critical as well as the protection used. It was found that the solid-state tap changers designed which are operational, these make use of transformers to provide the required voltage taps for the solid-state switches, as a result, lowers the voltage requirement of the switches. Two solid-state topologies were discussed; firstly, the thyristor-based solid-state tap changer, secondly, the IGBT-based solid-state tap changer. The discussion revealed that the IGBT-based solid-state tap changer contains numerous advantages, including, improved voltage regulation accuracy, faster reaction to sudden voltage changes. It is for these reasons that the solid-state tap changer designed in this thesis make use of IGBTs.

11.2 Hardware

The chosen layout of the IGBTs was presented in Chapter 2, this layout basically consisted out of two synchronous buck converters. These were connected to operate separately from each other; one converter operates during the positive half-cycle while the other operates during the negative half-cycle. This method of operation, however, requires a more sophisticated switching scheme than used for a normal synchronous buck converter.

The analysis conducted on the selection of the specific IGBT model in Chapter 5, revealed that the IGBTs are required to switch a peak voltage of

899 V. This relatively low voltage allowed the 1 700 V IGBT manufactured by Semikron to be used. This decision was based on the following factors; namely, the switching losses of the 1 700 V IGBT was the lowest while being the least expensive IGBT available. The low switching losses allows the IGBT-based tap changer to switch a 10 kHz, as a result, makes the inductance of the output filter inductor smaller.

The design of the passive components conducted in Chapter 5, included the following, the filter capacitors, the filter inductor as well as the snubber capacitor revealed that the values calculated for the components were realisable in practice.

The supporting hardware of the IGBT-based tap changer was discussed in Chapter 6. These PC-boards provide power to components and generates the signals used to control the IGBT-based tap changer. Most of these boards were designed and built prior to the start of the project for use on scale-model IGBT-based tap changer. It was revealed that the most crucial board is the sign detector. This board measures the polarity of the voltage over the IGBT and informs the controller of its status. This is used by the controller to generate the gating signals for the IGBTs, consequently, if the signal is incorrect, may damage the IGBTs.

11.3 Simulation and practical testing

The simulation results presented in Chapter 8 was used to verify the concept of the IGBT-based tap changer. It was found that the effect that the switching scheme has on the snubber capacitor was more than expected. The exclusion of the snubber capacitor during the negative half-cycle of the tap voltage, resulted in non-ideal filtering of the tap voltage. However, the other simulation results of the switching scheme as well as the filtering of the output voltage and current, has proven that the concept of the IGBT-based tap changer works as expected.

The practical measurements conducted on the scale-model IGBT-tap changer was presented in Chapter 9. The scale-model IGBT-based tap changer was built prior to the design of the full-size IGBT-based tap changer. The scale-model provided valuable information regarding the concept used for the IGBT-based tap changer. The measurement results also verified that the switching scheme presented works as expected. The result, however, was that the scale-model IGBT-based tap changer was able to regulate its output voltage with the specifically design controller.

11.4 Feedback controller

The feedback controller designed in Chapter 7 was designed not only to regulate the output voltage, but as well correct the output voltage waveform of the IGBT-based tap changer. The controller was mainly designed for the IGBT-based tap changer, however, it was tested on the scale-model IGBT-based tap changer and results gathered showed that the controller is capable of performing as desired.

11.5 Conclusions

The design objective for this project as presented in Section 1.4 in Chapter 1 have been reached and the following conclusions can be made:

- The best topology for the application of the IGBT-based tap changer onto a commercially available autotransformer was selected.
- The required hardware, software and controller was designed.
- The entire system was simulated in Simplorer and the concept of the IGBT-based tap changer was proven for MV applications.
- The IGBT-based tap changer concept was tested in practice and was found to be practically implementable.

11.6 Future work

This thesis presented the design of a MV IGBT-based solid-state tap changer that would be capable of regulating the output voltage of the tap changer to a much higher degree than would be possible by using mechanical tap changers. Although the concept has been tested on the scale-model tap changer and although it has been proven to work, this was not at the same voltage levels as for the full-scale IGBT-based tap changer. Consequently, it would still be necessary to build the IGBT-based tap changer designed in this thesis, and to test it thoroughly while operating at the voltages it was designed for in order to verify the design.

Appendices

Appendix A

Compensator design for the scale-model IGBT-based tap changer

This appendix discusses the design of the compensator for the scale-model IGBT-based tap changer. To begin, the transfer function of the scale-model IGBT-based tap changer is presented in (A.1):

$$\frac{V_{Load}(s)}{D(s)} = v_t R_O \Bigg(\frac{1}{C_1 C_2} + s^3 L_1 R_{C_2} + s^2 \Bigg(R_{C_2} \Big(R_{C_2} + R_{L_1} \Big) + \frac{L_1}{C_2} \Bigg) + s \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) \Bigg)$$

$$\frac{}{s^4 \Bigg[L_O L_1 \Big(R_O + R_{C_2} \Big) \Bigg]}$$

$$+ s^3 \Bigg[L_1 \Big(R_O R_{C_2} + R_O R_{L_O} + R_{C_2} R_{L_O} \Big) + L_O \Bigg(R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_2} + R_O \Big(R_{C_1} + R_{L_1} + R_{C_2} \Big) \Bigg) \Bigg]$$

$$+ s^2 \Bigg[R_O \Bigg(L_O \frac{C_1 + C_2}{C_1 C_2} + R_{L_O} \Big(R_{C_1} + R_{L_1} + R_{C_2} \Big) + R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_1} \Bigg) + L_O \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) + R_{L_O} \Bigg(R_{C_2} \Big(R_{C_1} + R_{L_1} \Big) + \frac{L_1}{C_1} \Bigg) \Bigg]$$

$$+ s \Bigg[R_O \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} + R_{L_O} \frac{C_1 + C_2}{C_1 C_2} \Bigg) + R_{L_O} \Bigg(\frac{R_{C_2} C_2 + R_{C_1} C_1 + R_{L_1} C_1}{C_1 C_2} \Bigg) + \frac{L_O}{C_1 C_2} \Bigg]$$

$$+ \Bigg[\frac{R_O + R_{L_O}}{C_1 C_2} \Bigg] \tag{A.1}$$

Table A.1 lists all the values of the variables for the transfer function of the scale-model IGBT-based tap changer in (A.1).

The load resistance is taken at 211.6 Ω, allowing the compensator to be designed for a load of 5 % of the full rated load resistance.

Drawing the root locus of the plant in Figure A.1, as based on the provided variables, shows that the plant has two sets of complex poles and one complex zero. The two complex poles require a proportional-integral derivative (PID) controller with a high frequency pole [30] shown in (A.2) to be used to control the output voltage of the plant. The compensator implements a complex zero, which is used to compensate for a complex pole pair in the system.

$$C(s) = G_{cp} \frac{s + \omega_z}{s(s + \omega_p)} \tag{A.2}$$

Description	**Symbol**	**Value**
Transformer winding leakage inductance	L_1	24.107 μH
Filter capacitors	C_1 and C_2	100 μF
Output filter inductor	L_O	488.9 μH
Tap voltage	v_t	56.56 V
Series resistance of transformer winding	R_{L_1}	0.008 Ω
Equivalent series resistance of capacitors	R_{C_1} and R_{C_2}	0.005 Ω
Equivalent series resistance of output inductor	R_{L_O}	0.03 Ω
Load impedance	R_O	211.6 Ω

Table A.1: Values of variables used in for the derived mathematical model of the scale-model IGBT-based tap changer.

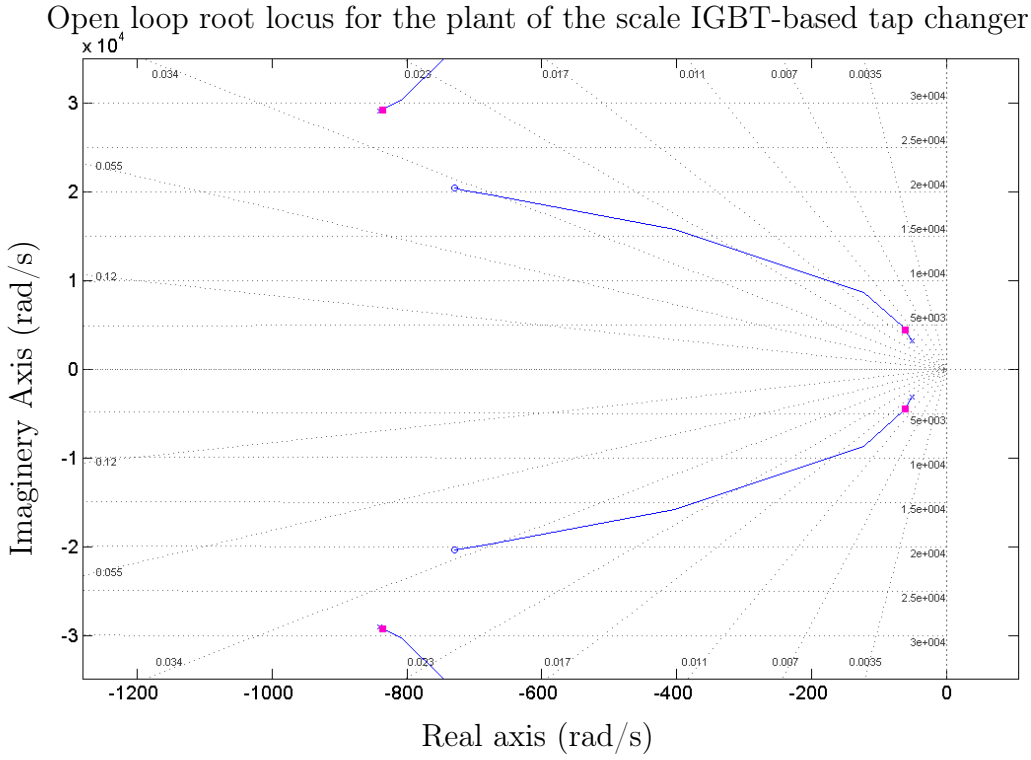

Figure A.1: Root locus plot of the open loop system for the scale-model IGBT-based tap changer without compensation.

It is necessary to know the position of each of the poles in order to select which pole to compensate for. The positions of the two complex poles are shown in (A.3) and (A.4).

$$s_1 = -840.642 \pm j29\ 034\ rad/s \tag{A.3}$$

$$s_2 = -52.113 \pm j3\ 178.05\ rad/s \tag{A.4}$$

Table A.2 provides the natural frequency and damping ratio for both poles, calculated with (A.5) and (A.6), with x the real part of the pole position and y the imaginary part.

$$\omega_n = \sqrt{x^2 + y^2} \tag{A.5}$$

$$\zeta = \frac{|x|}{|y|} \tag{A.6}$$

Description	Symbol	Value
Natural frequency of pole s_1	ω_{n_1}	29 046.17 rad/s
Damping ratio for pole s_1	ζ_1	0.028 954
Natural frequency of pole s_2	ω_{n_2}	3 178.48 rad/s
Damping ratio for pole s_2	ζ_2	0.016 397

Table A.2: Natural frequency and damping ratio for each of the two poles.

The natural frequency of pole s_1 is too fast for the compensator to compensate for with the switching frequency of the scale-model IGBT-based tap changer at 62 831.85 rad/s. Consequently, the compensator must be designed to compensate for the second complex pole s_2. The design of the complex zero in the compensator is to have a natural frequency 30% smaller than that of the complex pole, while the damping ratio of the zero is twice the value of the pole. This results in the zero to having a natural frequency of 2 224.94 rad/s with a damping ratio of 0.032 795. The resulting position of the complex pole is given in (A.7).

$$s_z = -72.967 \pm j2\ 223.74\ rad/s \tag{A.7}$$

The next component of the compensator that must be designed is the high frequency pole. This is designed so that the resulting plant with the compensator added has a cut-off frequency of $\omega_{0dB} = 6\ 283$ rad/s with a phase margin $\phi_M = 57.5°$.

Using (7.2.4)[1] delivers the required phase of the compensator $\phi_{cp} = 54.29°$ with the converter phase ϕ_{cv} = -176.79°. Calculating the multiplication factor with (7.2.5)[2] results in the value of -1.950. Using this factor together with the calculated compensator frequency of the complex zero and the required cut-off

[1] See page 106
[2] See page 106

Open loop bode plot for the compensatoed scale IGBT-based tap changer

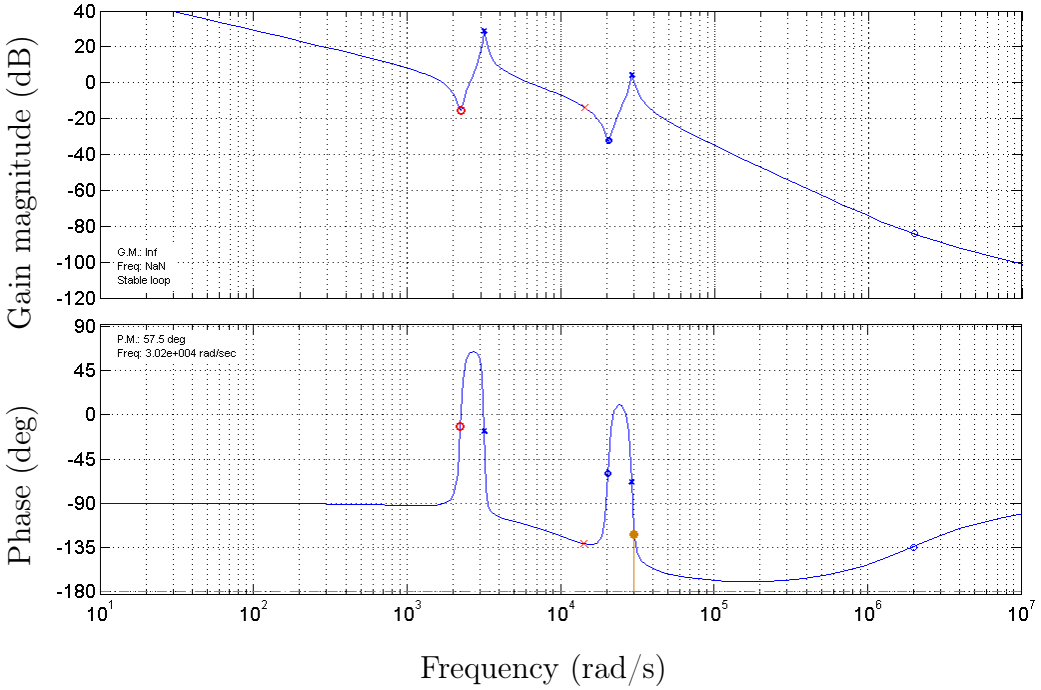

Figure A.2: Bode plot plot of the open loop system of the scale-model IGBT-based tap changer with compensation.

frequency of the plant in (A.8) mean that the high frequency pole must be placed at 14 223.01 rad/s.

$$\omega_p = \sqrt{\omega_{cp}\omega_{0dB}} f_{ct}^2 \tag{A.8}$$

The final value that needs to be calculated is the gain of the compensator. Using the sisotool application in Matlab allows the gain to be adjusted in real time, while the Bode plot is shown. Adjusting the gain until it reaches a value of 0.1485 results in the compensated plant having a cut-off frequency of 6 283 rad/s with the phase margin at 57.5° as shown in Figure A.2.

The resulting compensator is shown in (A.9) below:

$$C(s) = 0.1485 \frac{s^2 + 145.935s + 4950340}{s(s + 14\ 223.01)} \tag{A.9}$$

The resulting root locus analysis of the entire system with the compensator added is shown in Figure A.3.

The root locus shows that none of the loci goes into the right hand plane which allows the gain to be adjusted without limits.

Thereafter, the controller is designed by using the c2d function in Matlab with a sampling period of 0.000 1 s together with the tustin approximation. The result is shown in (A.10), and it can be implemented into the FPGA.

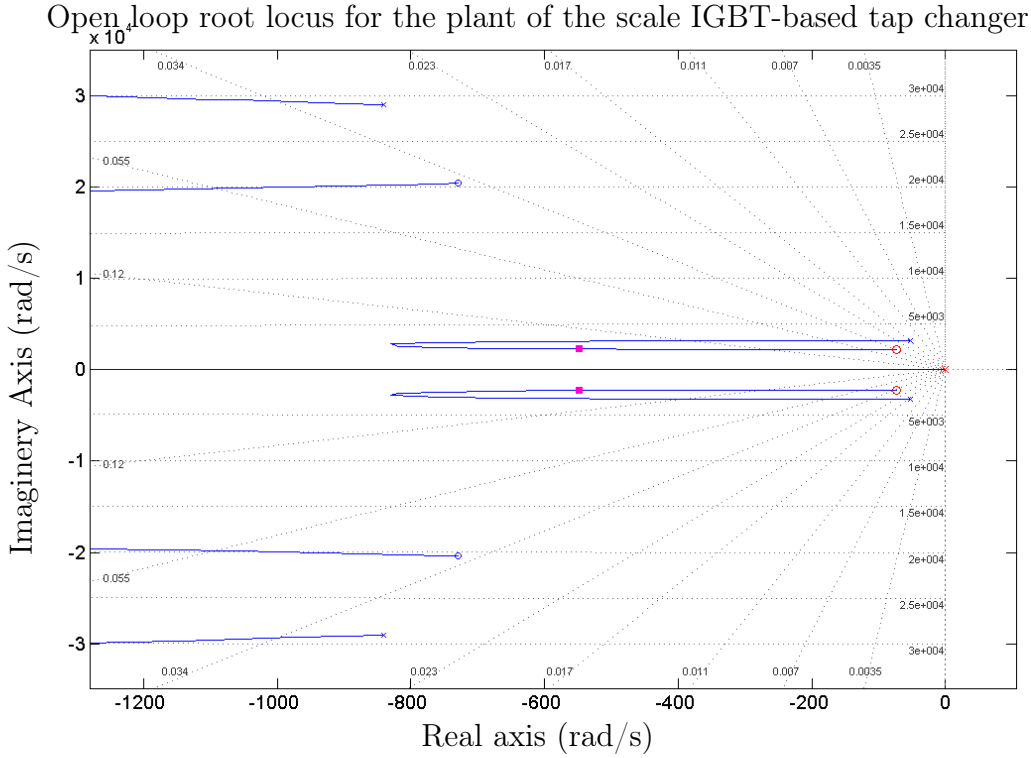

Figure A.3: Root locus plot of the open loop system for the scale-model IGBT-based tap changer without compensation.

$$C(z) = 0.088\ 41\frac{z^2 - 1.941z + 0.985\ 7}{z^2 - 1.169z + 0.168\ 8} \tag{A.10}$$

The gain of the compensator is determined for a peak tap voltage v_t of 56.56 V and provision must be made for the gain at lower voltages. Thus, multiplying the gain in (A.10) with 56.56 delivers a value of 5.000 47. Making the gain dynamic as stated in Chapter 7 is crucial to the success of the compensator, as it results in the compensator gain being divided by the tap voltage. The tap voltage is not measured but simulated in the FPGA by means of a waveform generator, which generates a sinusoidal waveform that can be used as the tap voltage measurement. The final compensator implemented in the FPGA is shown in (9.3.1) using the methods on page 110.

$$\begin{aligned} d(k) \quad = \quad & \frac{5.000\ 47}{v_t}\Big(error(k) - 1.941error(k-1) + 0.985\ 7error(k-2)\Big) \\ & +1.169d(k-1) - 0.168\ 8d(k-2) \end{aligned} \tag{A.11}$$

The compensator presented in (A.11) is used for the practical measurements.

List of References

[1] C. R. Bayliss, *Transmission and Distribution : Electrical Engineering*, 2nd ed. Newnes, 1999.

[2] E. Lefeuvre, T. Meynard, and P. Viarouge, "Robust Two-Level and Multilevel PWM AC Choppers," in *European Power Electronics and Drives Association (EPE) Conference*, Gratz, Austria, 2001, pp. 1–8.

[3] Cooper Power Systems, "VR-32 voltage regulator with quick-drive tap-changer, installation, operation and maintenance instructions (S255-10-30) data sheet," 2007.

[4] ESKOM, "MV electronic voltage regulator development," RSA, 2008.

[5] Electrical Power Research Institute (EPRI), "Evaluate solid state LTC options for medium power transformers," Palo Alto, CA, Tech. Rep. 41C3084/6658-6424, 2000.

[6] Altera, "Cyclone III device handbook,Volume 1," pp. 1–3, 2009.

[7] F. Yousef-Zai and D. O'Kelly, "Solid-state on-load transformer tap changer," *Electric Power Applications*, vol. 143, pp. 481–491, 1996.

[8] INFINEON, "FZ400R65KF2 IGBT-module Datasheet," 2008.

[9] P. Bauer, S. de Haan, and G. Paap, "Tap changer for 10kv distribution transformer: System lay-out and control," in *International Power Electronics and Motion Control Conference (IPEMC)*, Hangzhou, China, Novermber 1997, pp. 250–255.

[10] P. Bauer and S. de Haan, "Electronic tap changer for 500 kva / 10 kv distribution transformers : Design, experimental results and impact in distribution networks," in *IEEE Industry Applications Conference*, vol. 2, St.Louis, MO, USA, October 1998, pp. 1530–1537.

[11] J. Winders, *Power Transformers : Principles and Applications*, 1st ed. Marcel Dekker Inc., 2002.

[12] M. R. Spiegel and J. Liu, *Mathematical Handbook of Formulas and Tables*, 2nd ed. McGraw-Hill, 1999.

[13] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley & Sons Inc, 2003.

[14] J. W. Nilsson and S. A. Riedel, *Electric Circuits*, 7th ed. Upper Saddle River, New Jersey 07458, USA: Prentice Hall, 2005.

[15] B. S. Guru and H. R. Hiziroglu, *Electric Machinery and Transformers*, 3rd ed. Oxford University Press, 2001.

[16] T. Wildi, *Electrical machines, drivers, and power systems*, 6th ed. Prentice Hall, 2006.

[17] Cooper Power Systems, "Voltage regulating apparatus : Determination of regulator compensator settings (R255-10-1)," 2003.

[18] MITSUBISHI, "CM400HB-90H IGBT-module Datasheet," 2003.

[19] EUPEC, "FZ400R33KL2C_B5 IGBT-module Datasheet," 2004.

[20] SEMIKRON, "SKM 600GA176D IGBT-module Datasheet," 2006.

[21] SEMIKRON, "PX16 Heat sink Datasheet," 2005.

[22] Electricity Council Great Britain, Ed., *Power System Protection Volume 1: Principles and components*, 2nd ed. The Institution of Electrical Engineers, London, 1995.

[23] SEMIKRON, "SKET 740 Thyristor Datasheet," 2008.

[24] EPCOS, "EPCOS MKV AC capacitors : General AC applications," 2005.

[25] National Semiconductor, "LM311 datasheet," 2001.

[26] IXYS, "Breakover diodes datasheet," 2000.

[27] Liaisons Electroniques-Mécaniques(LEM), "LV100-4000/SP12 Datasheet," 2003.

[28] Liaisons Electroniques-Mécaniques(LEM), "LF 205-S Datasheet," 2008.

[29] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback control of Dynamic Systems*, 4th ed. Upper Saddle River, New Jersey 07458, USA: Prentice Hall, 2002.

[30] M. H. Rashid, *Power electronics handbook : Devices, circuits, and applications*, 2nd ed. 30 Corporate Drive, Suite 400, Burlington, MA 01803, USA: Academic Press, 2007.

[31] Analog Devices, "AD7924 datasheet," 2002.